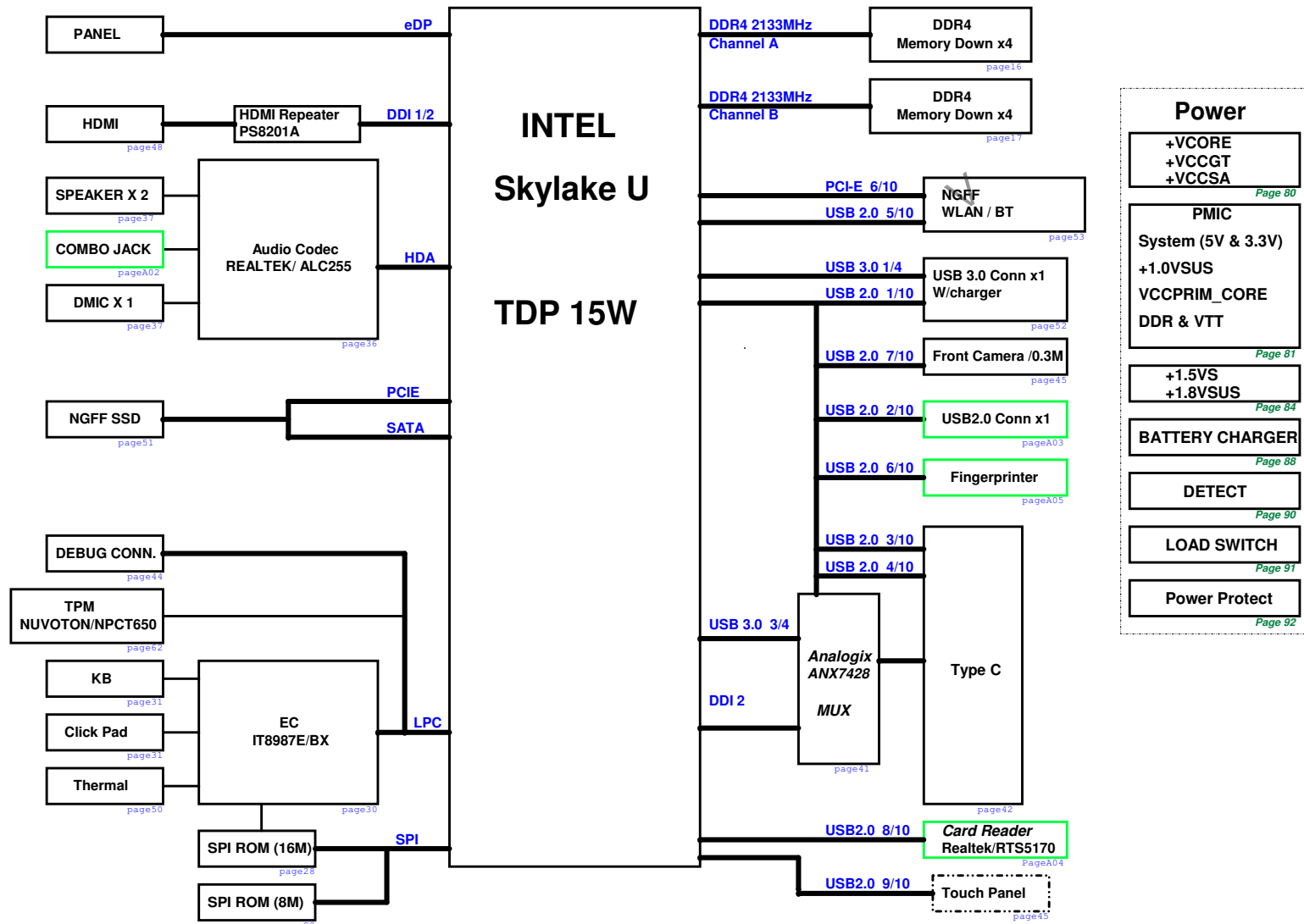


14" Cassiopeia (X3) for Skylake U Platform Block Diagram



www.schematic-x.blogspot.com

Discharge Circuit

Page 57

DC & BATT. Conn.

Page 60

Reset Circuit

Page 32

Skew Holes

Page 65

<Variant Name>

PEGATRON Title : Block Diagram
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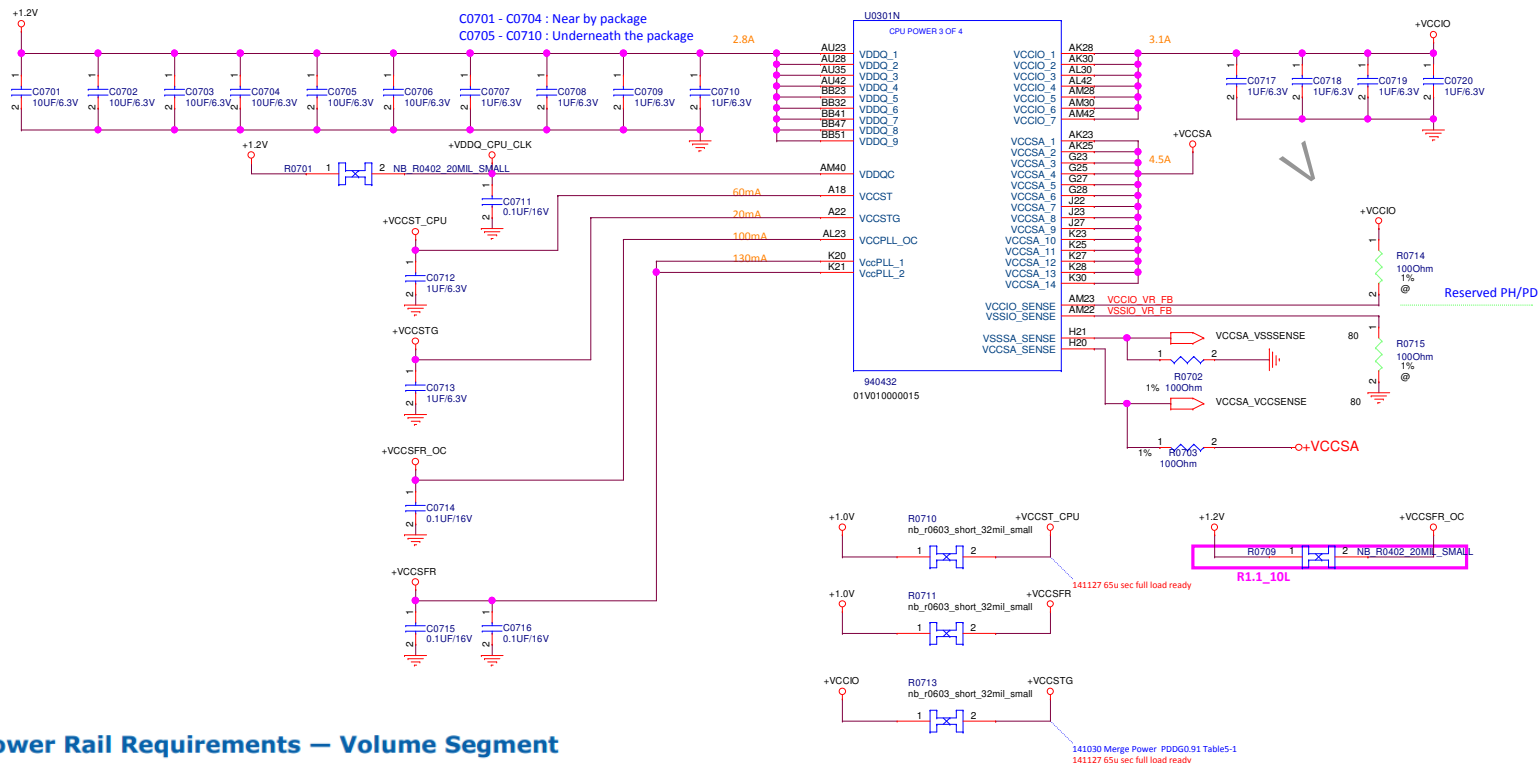
BGI/HW3 Engineer: Andy Kao

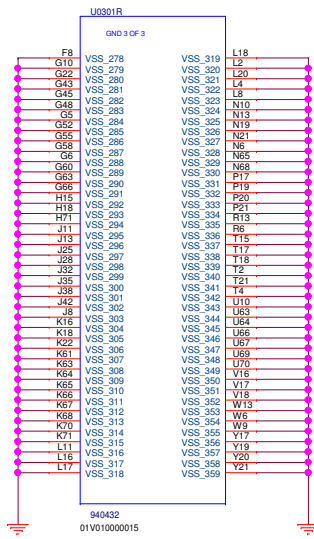
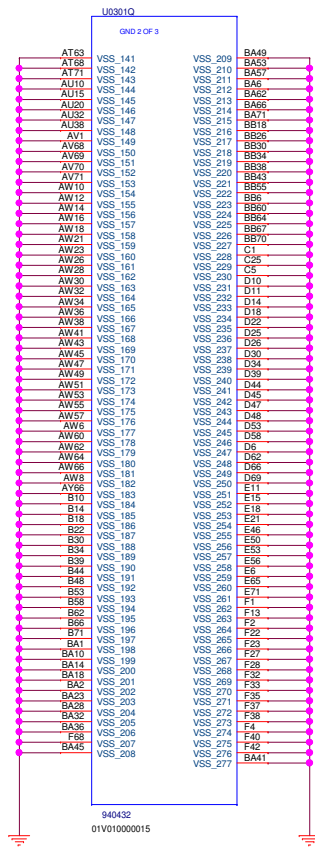
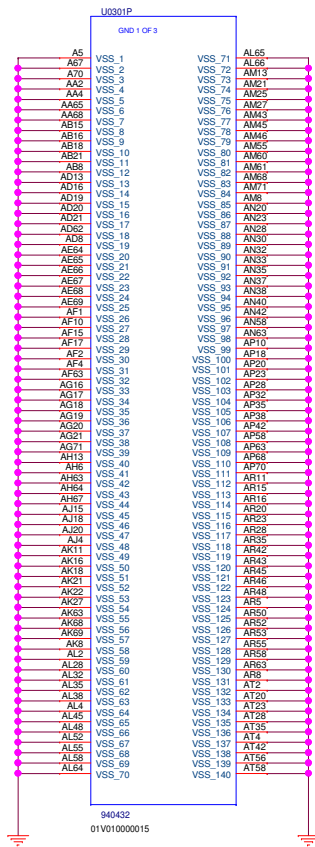
Size Project Name
Custom X3 Rev 1.0

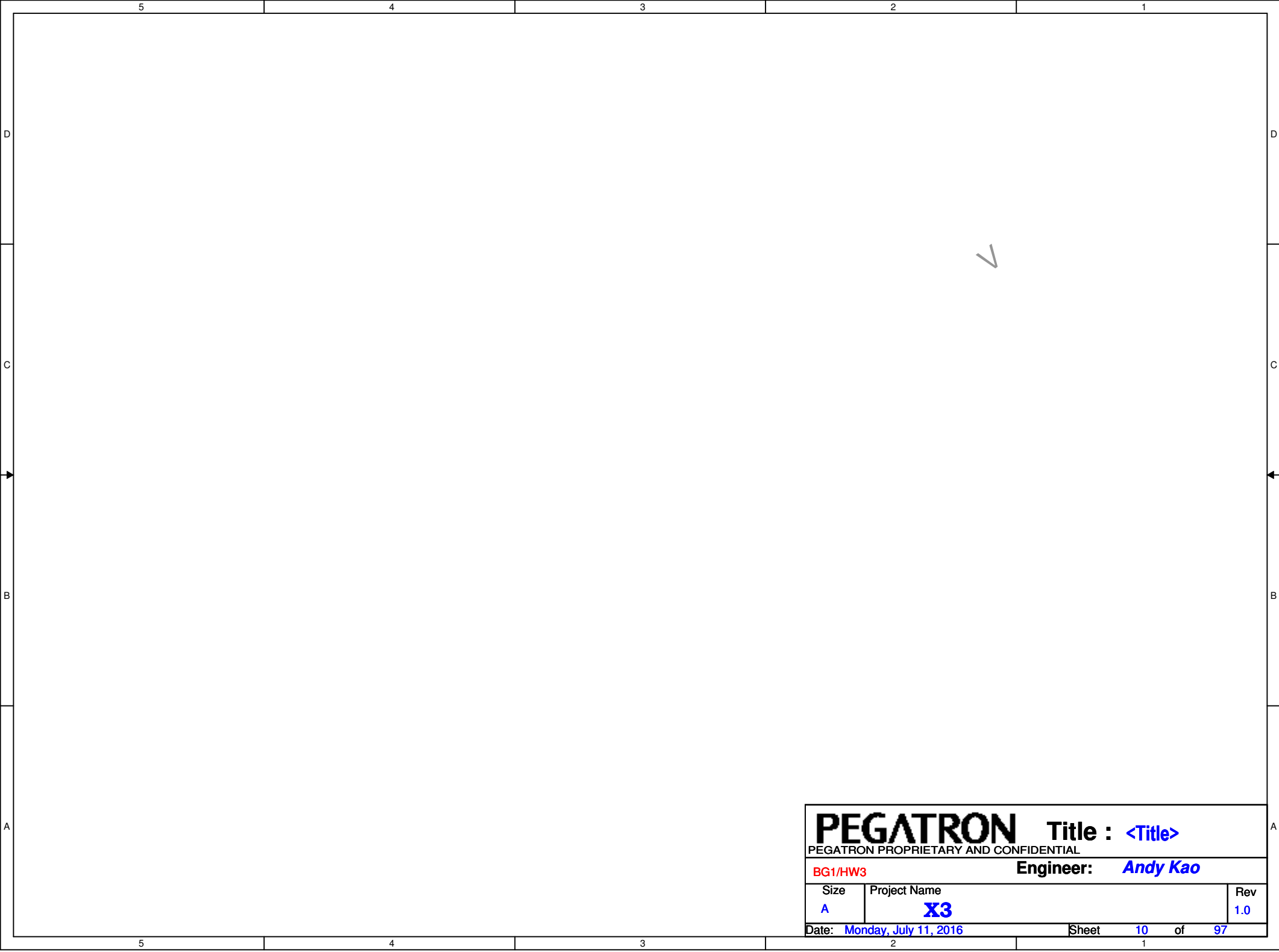
Date: Monday, July 11, 2016 Sheet 1 of 97

5			4			3			2			1														
EC GPIO			Use As			Signal Name			EC GPIO			Use As			Signal Name			EC GPIO			Use As			Signal Name		

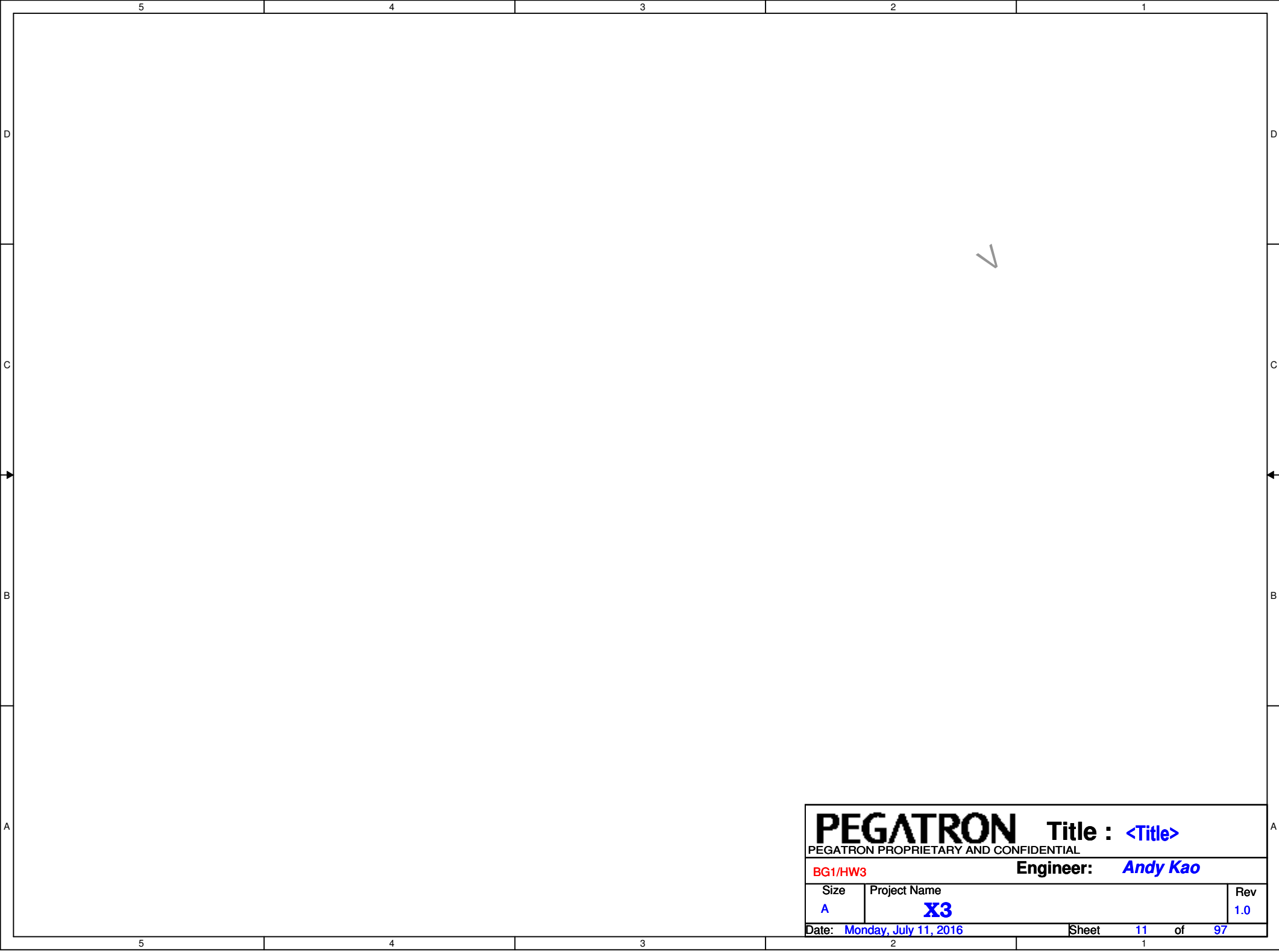




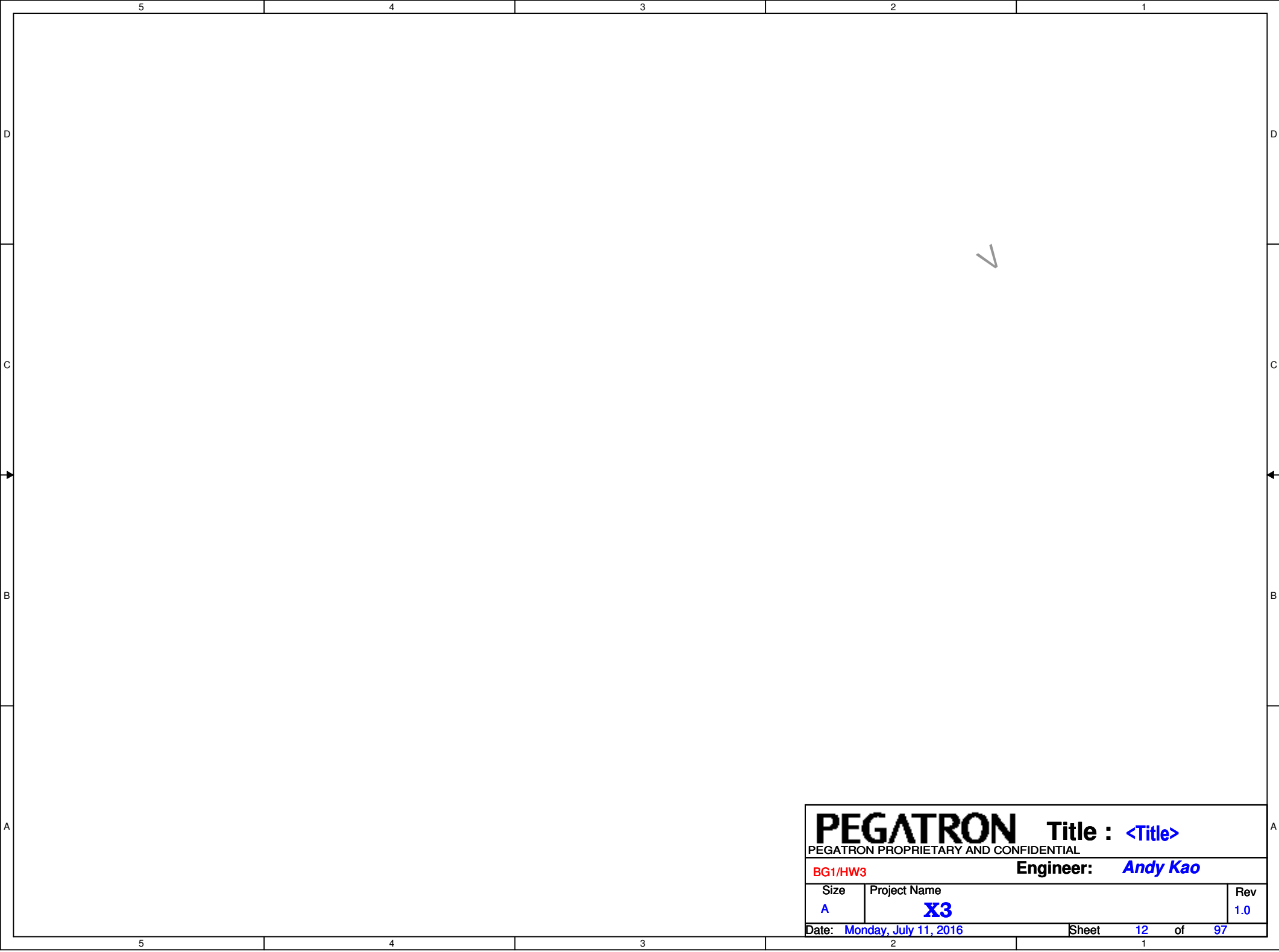




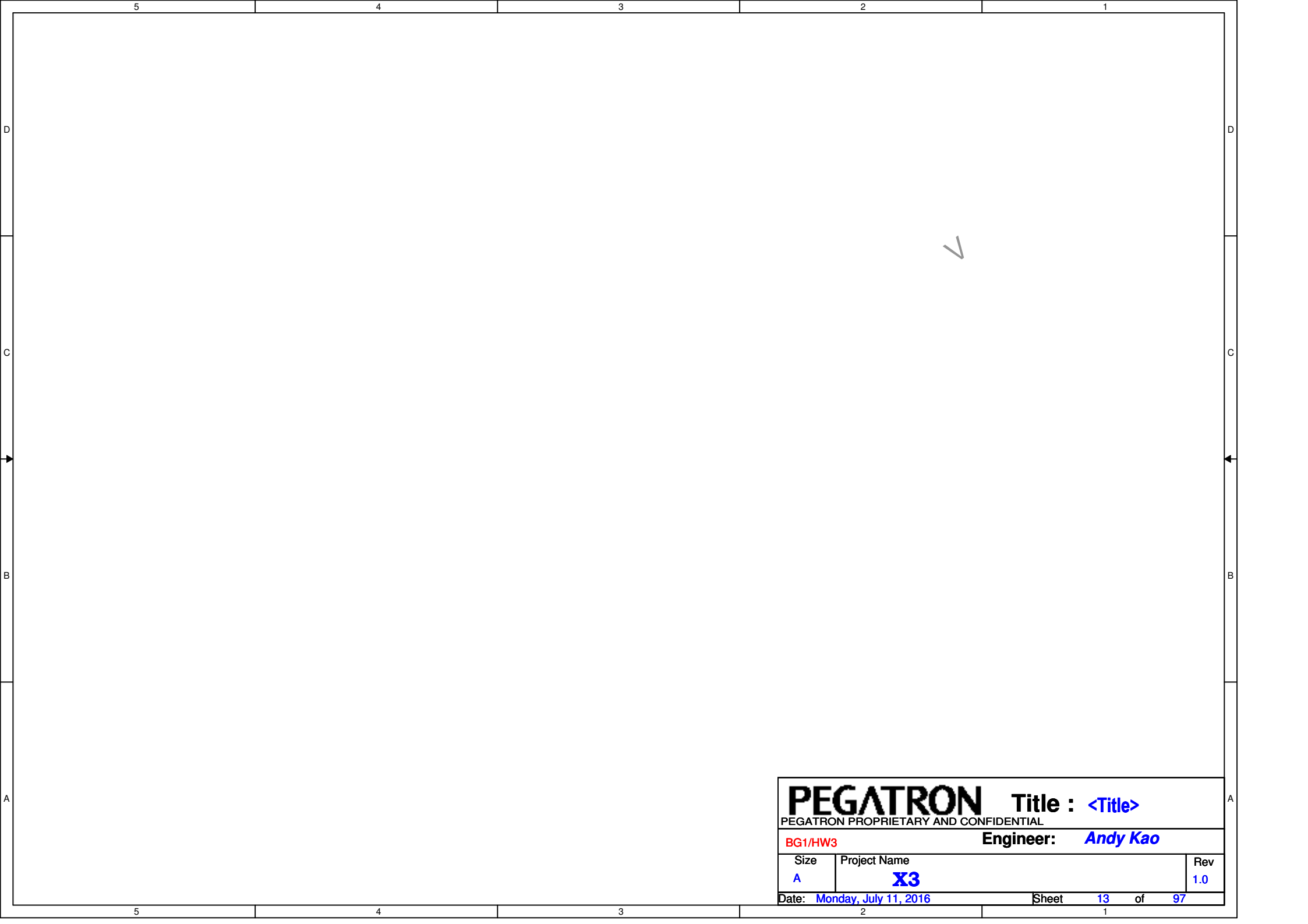
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 10 of 97	



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BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
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Size A	Project Name X3	Rev 1.0
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D

D

C

C

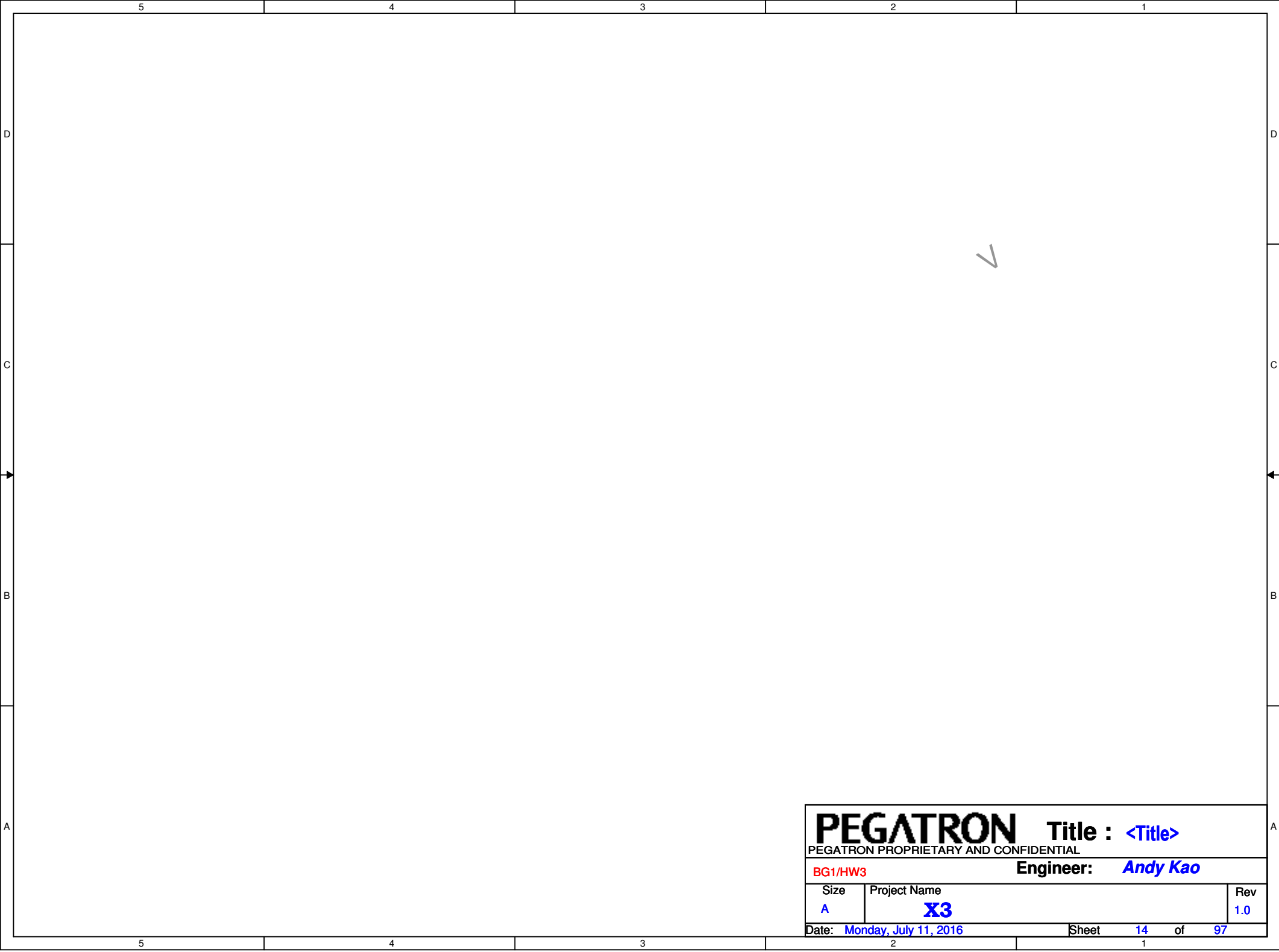
B

B

A

A

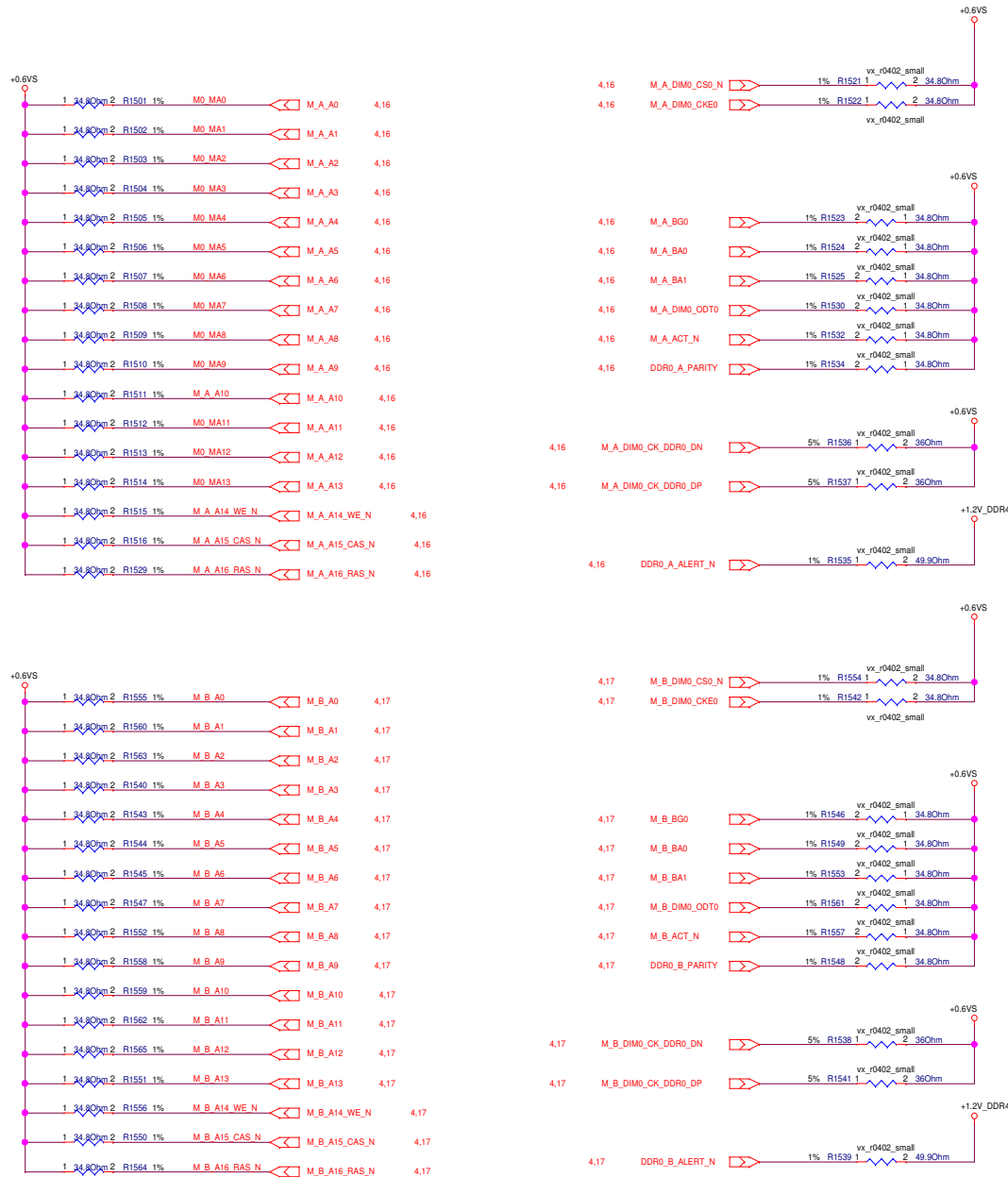
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BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
Date: Monday, July 11, 2016			Sheet	13	of 97



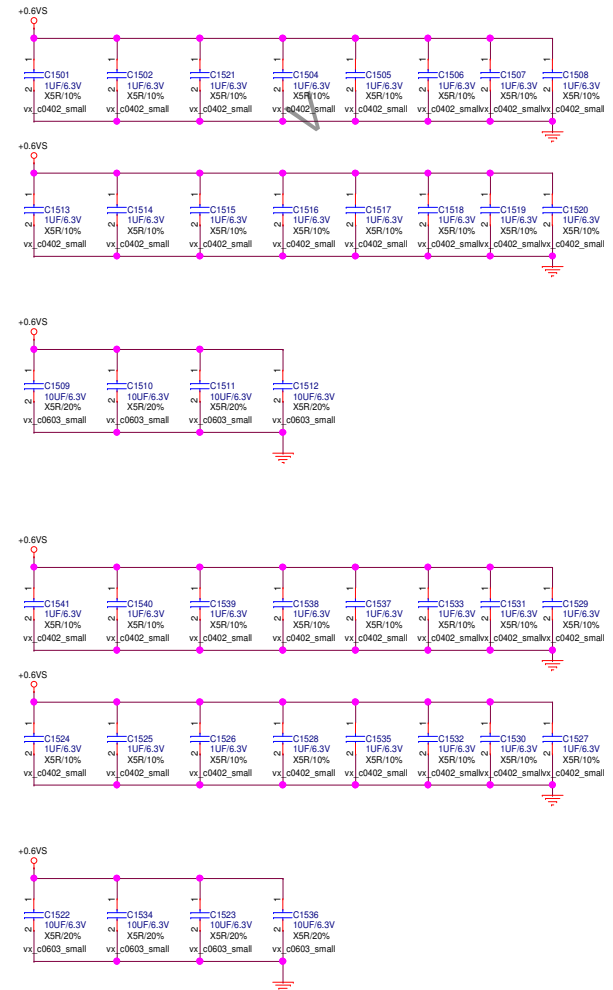
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BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>14</i> of <i>97</i>

DDR4(0)_Termination

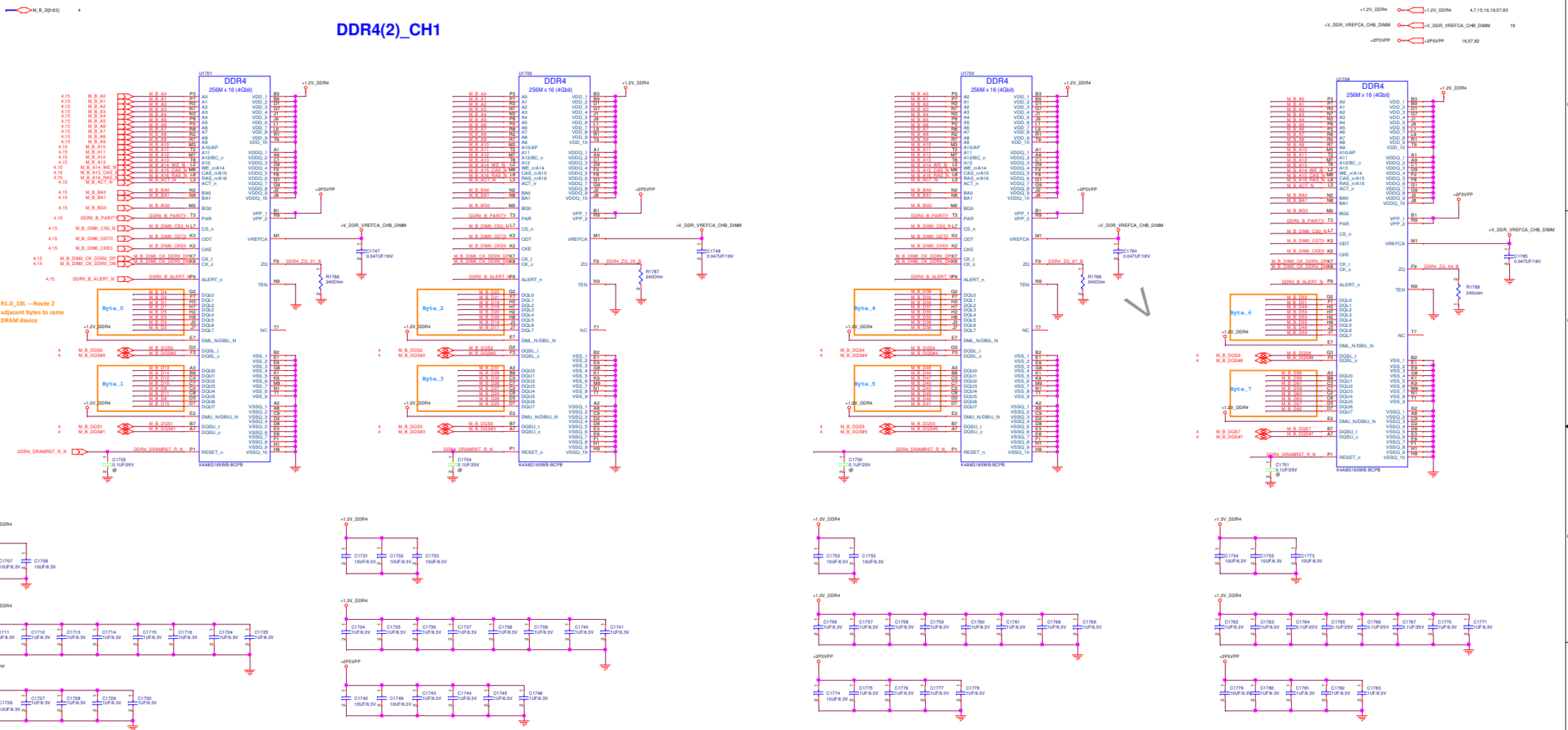
+0.6VS 57.83
+1.2V_DDR4 4.7,16,17,19,57,83

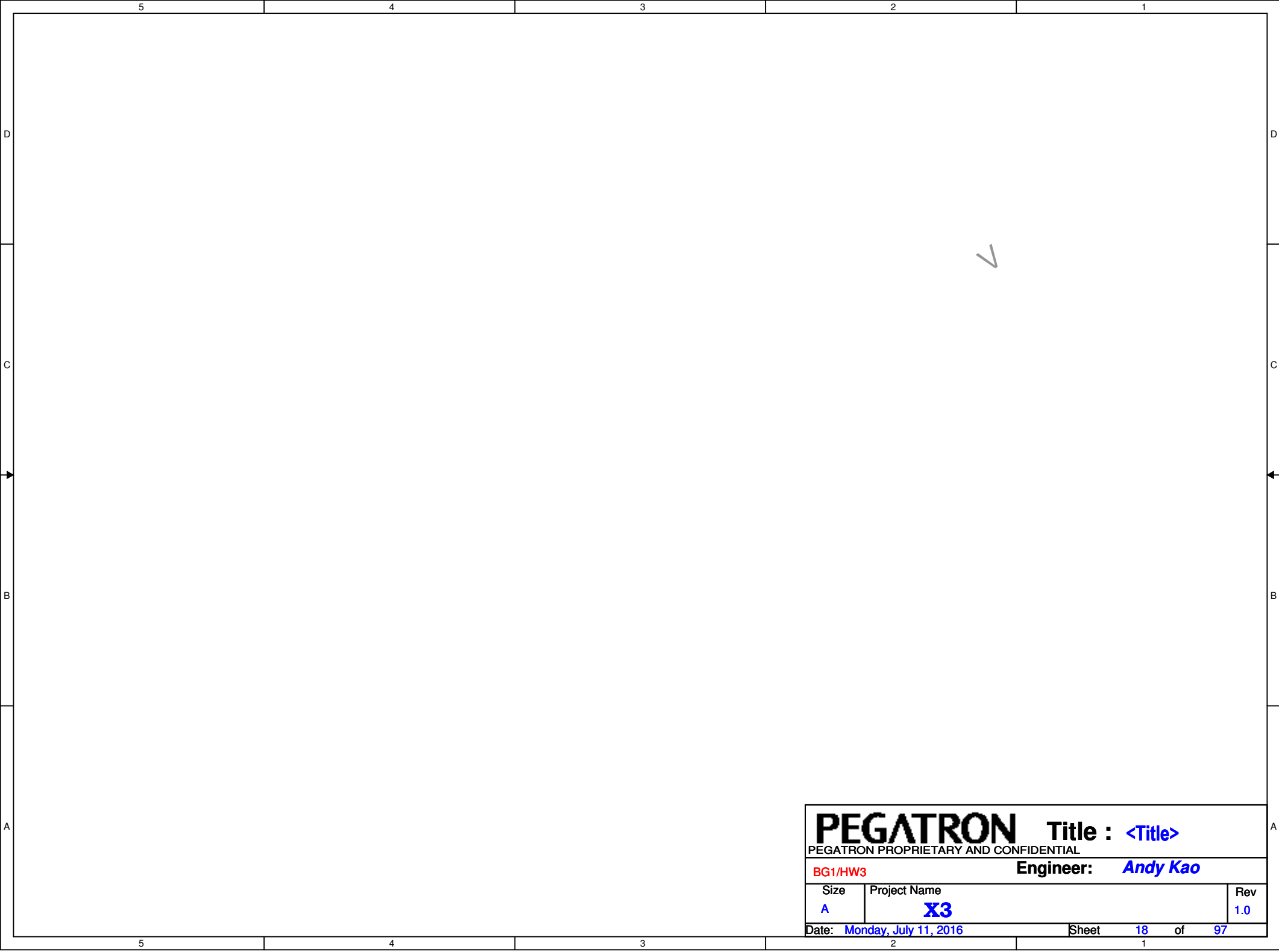


Average placed close to +VDDQ_VTT power plane










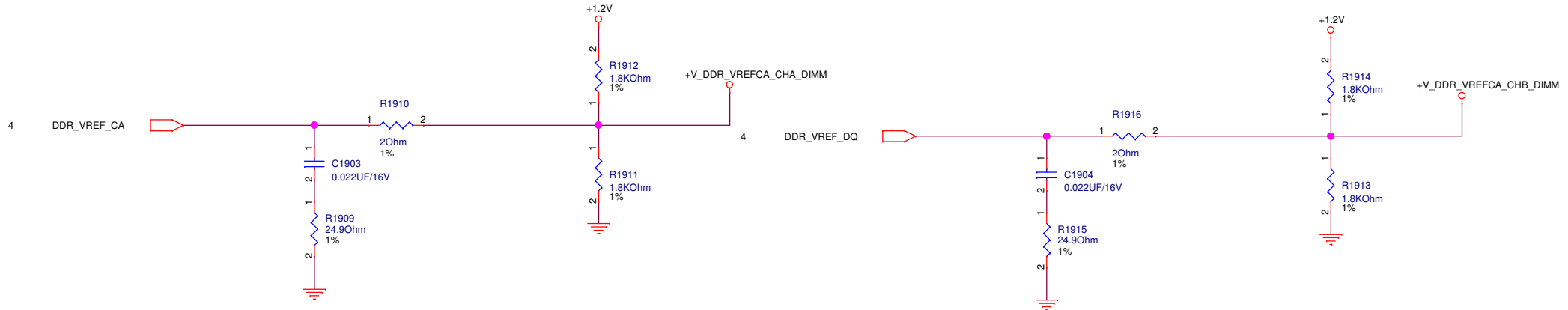


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BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
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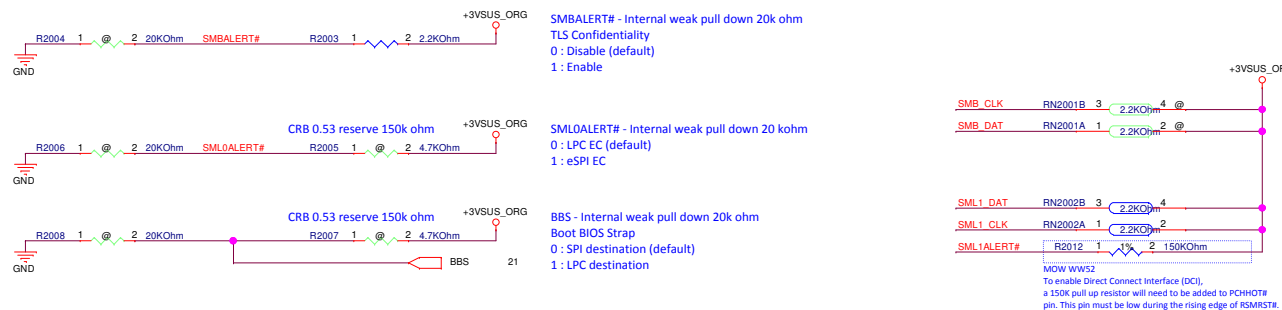
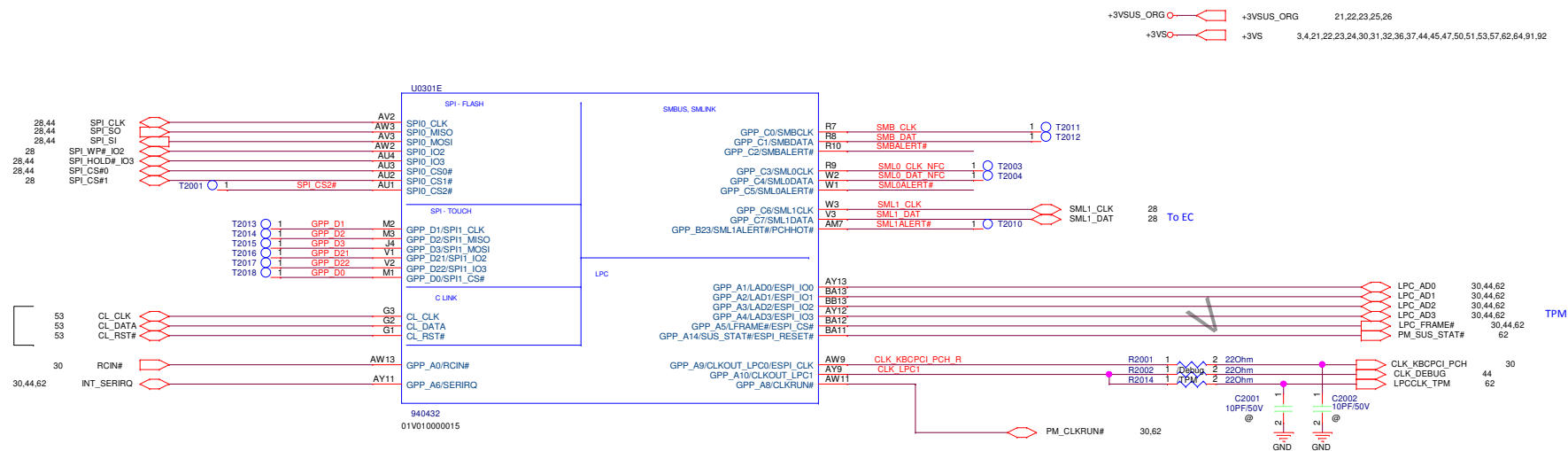
DDR4(3)_CA/DQ Voltage

+1.2V		+1.2V	4,7,15,16,17,57,83
+V_DDR_VREFCA_CHB_DIMM		+V_DDR_VREFCA_CHB_DIMM	17
+V_DDR_VREFCA_CHA_DIMM		+V_DDR_VREFCA_CHA_DIMM	16

DDR4 Vref (Intel Schematic Review)

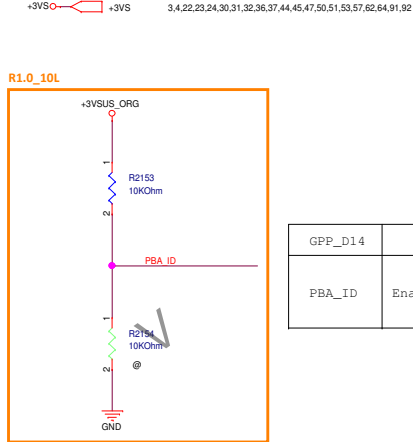
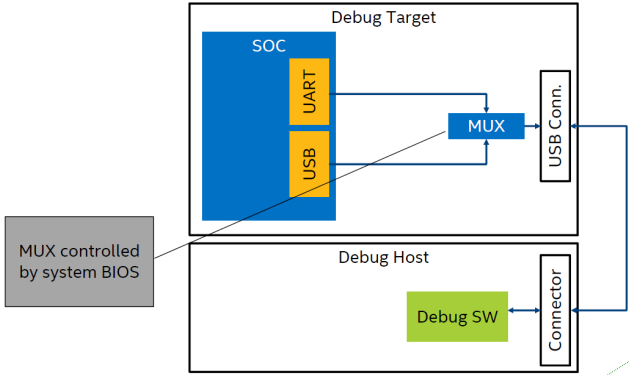


<Variant Name>		
PEGATRON Title : DDR3(3)_CA/DQ Voltage		
BG1/HW3 Engineer: Andy Kao		
Size B	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016 Sheet 19 of 97		

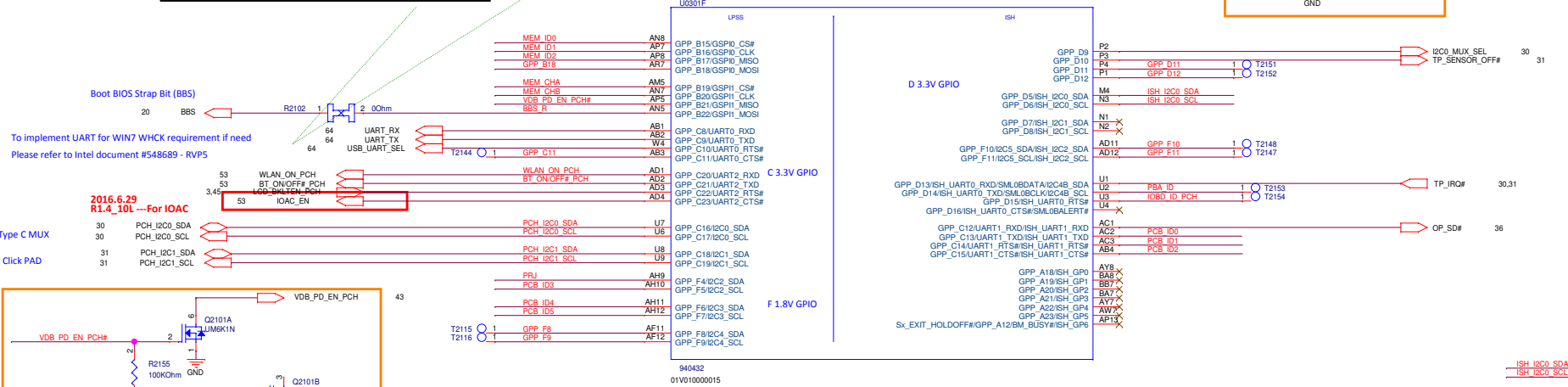


Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port. With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required

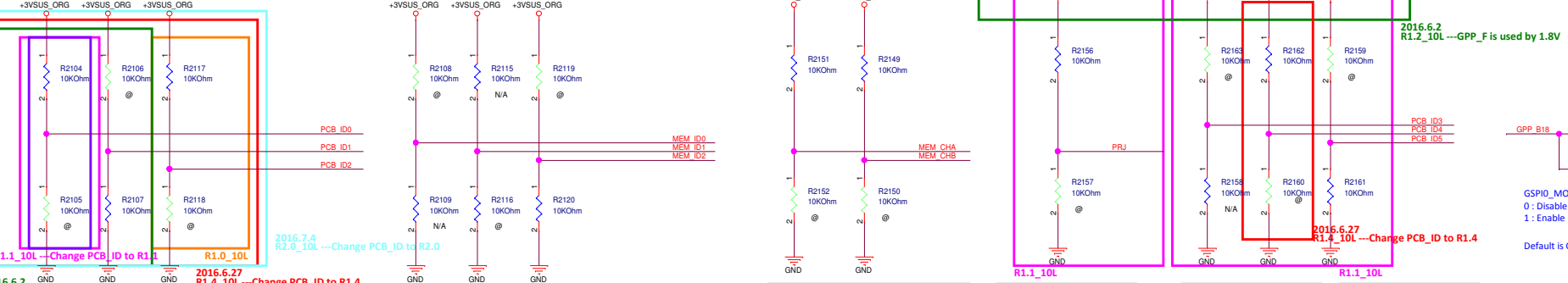
COMPRESSED IMAGE



GPP_D14	1	0
PBA_ID	Enable	Disable



R1.0_10L ---Follow HAWAII type-c design



2016.6.2 R1.2_10L ---Change PCB_ID to R1.2
2016.6.14 R1.3_10L ---Change PCB_ID to R1.3
2016.6.27 R1.4_10L ---Change PCB_ID to R1.4

MB Version ID

PCB_ID4 (GPP_F6)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)	PCB_ID2 (GPP_C15)	MEM_ID1 (GPP_B16)	MEM_ID2 (GPP_B17)	MEM_ID0 (GPP_B15)
R1.0	0	0	8L	4Gb	0	0
R1.1	0	0	10L	8Gb	1	0
R1.2	0	1				1
R1.3	0	1				0
R1.4	1	0				0
R2.0	1	0				1

Memory ID

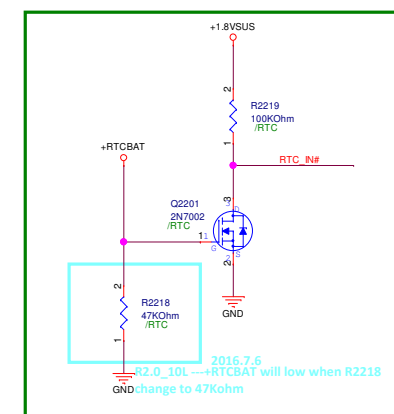
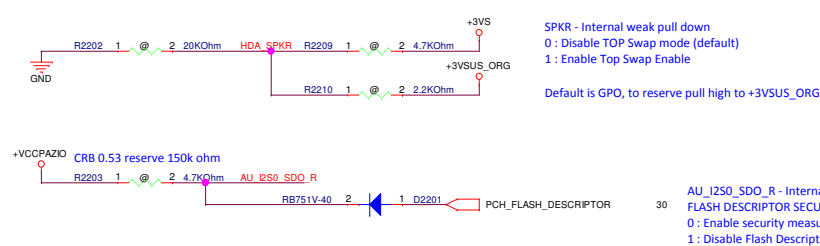
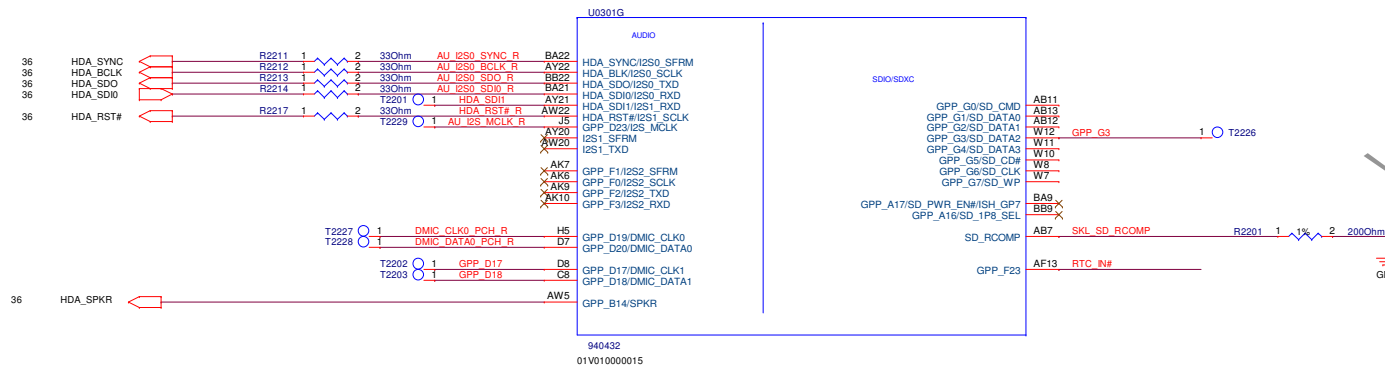
PCB_ID2 (GPP_C15)	MEM_ID1 (GPP_B16)	MEM_ID2 (GPP_B17)	MEM_ID0 (GPP_B15)
8L	0	0	0
10L	1	1	0
			1

	CHA	CHB
GPP_B19 (0)	Disable	
GPP_B19 (1)	Enable	
GPP_B20 (0)		Disable
GPP_B20 (1)		Enable

	PRJ
GPP_F4 (0)	M3
GPP_F4 (1)	X3

	PCB_ID3
GPP_F5 (0)	SKL
GPP_F5 (1)	KBL

	PCB_ID5
GPP_F7 (0)	2133
GPP_F7 (1)	2400



2016.5.11
R1.2_10L ---RTC detect circuit

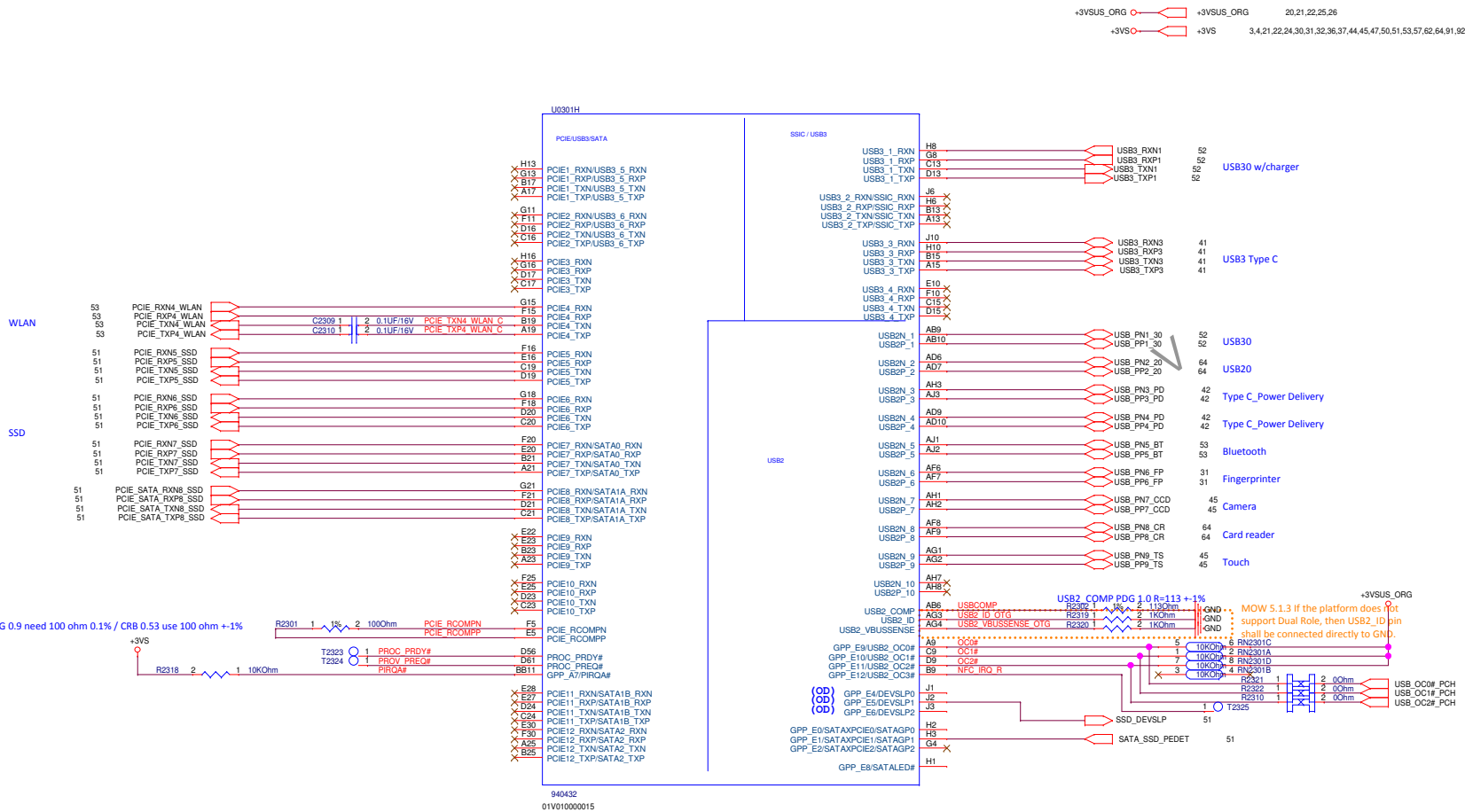


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Internal RST capable PCIe and SATA Express* Storage Devices	0	2	2
Notes: 1. USB 2.0 port numbers: 1-8 2. USB 2.0 port numbers: 1-10 3. USB 2.0 port numbers: 1-6 4. SATA Express Capable Ports (x2)			

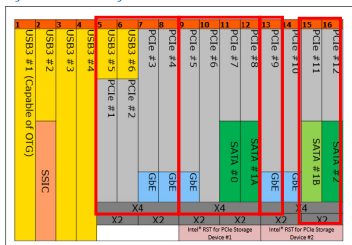
Table 1-3. PCH-LP HSI0 Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0 OTG	USB 3.0 OTG	USB 3.0 OTG	USB 3.0 OTG	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	SATA	PCIe	PCIe	N/A	N/A
Premium-U	USB 3.0 OTG	USB 3.0 OTG	USB 3.0 OTG	USB 3.0 OTG	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe
Premium-Y	USB 3.0 OTG	USB 3.0 OTG	USB 3.0 OTG	USB 3.0 OTG	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1.0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSI0 Muxing on SKL PCH U



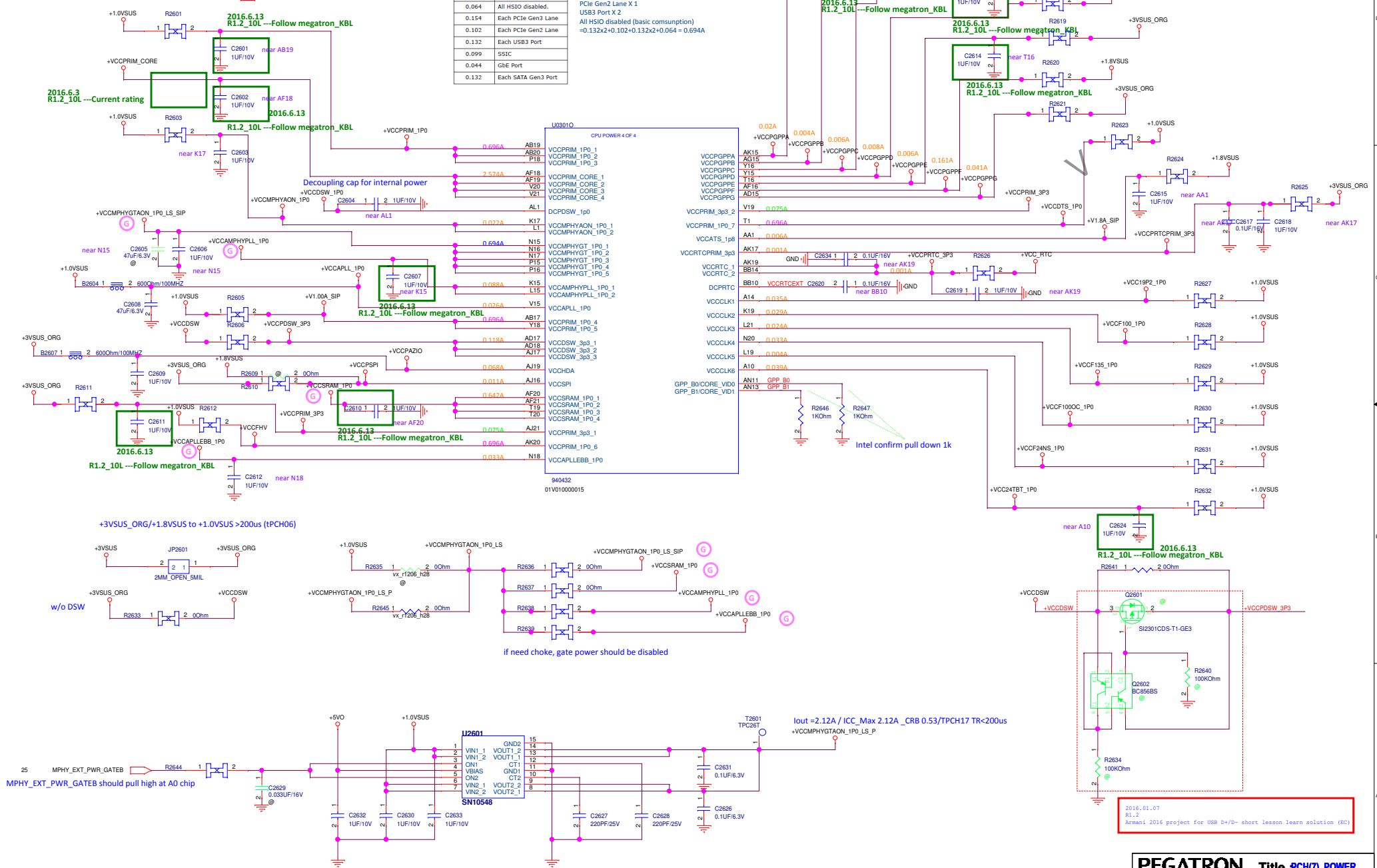
CONFIDENTIAL

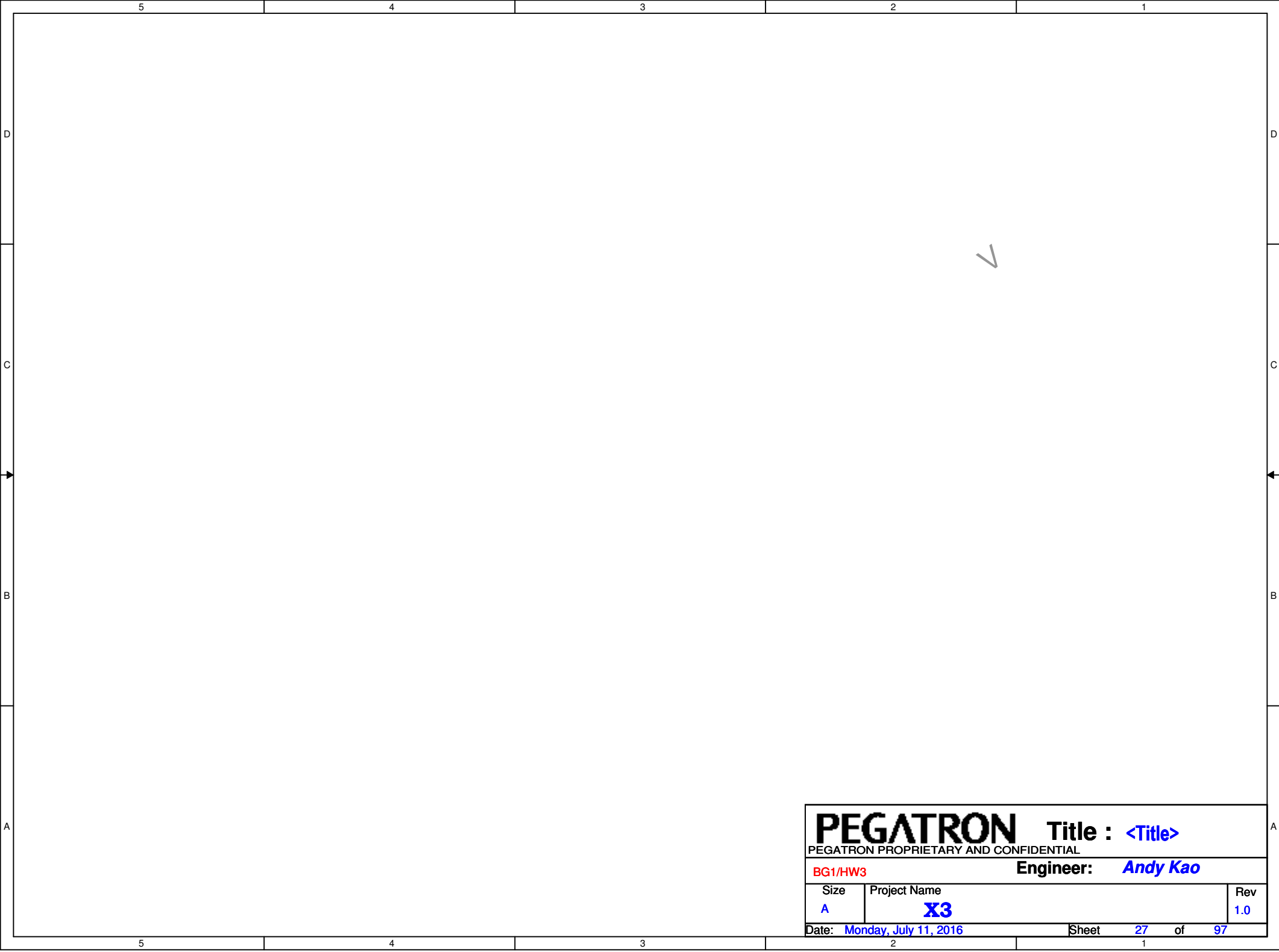
+1.0VSUS	82
+VCCDSW	25,30
+1.8VSUS	9,21,22,84
+VCCPAZIO	22
+VCC_RTC	24,25,36,60
+VCCF24NS_1P0	+VCCF24NS_1P0 24
+3VSUS_ORG	+3VSUS_ORG 20,21,22,23,25
+3VSUS	4,24,25,28,30,31,41,42,51,53,62,64,68,81,92

Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSI0 Lane

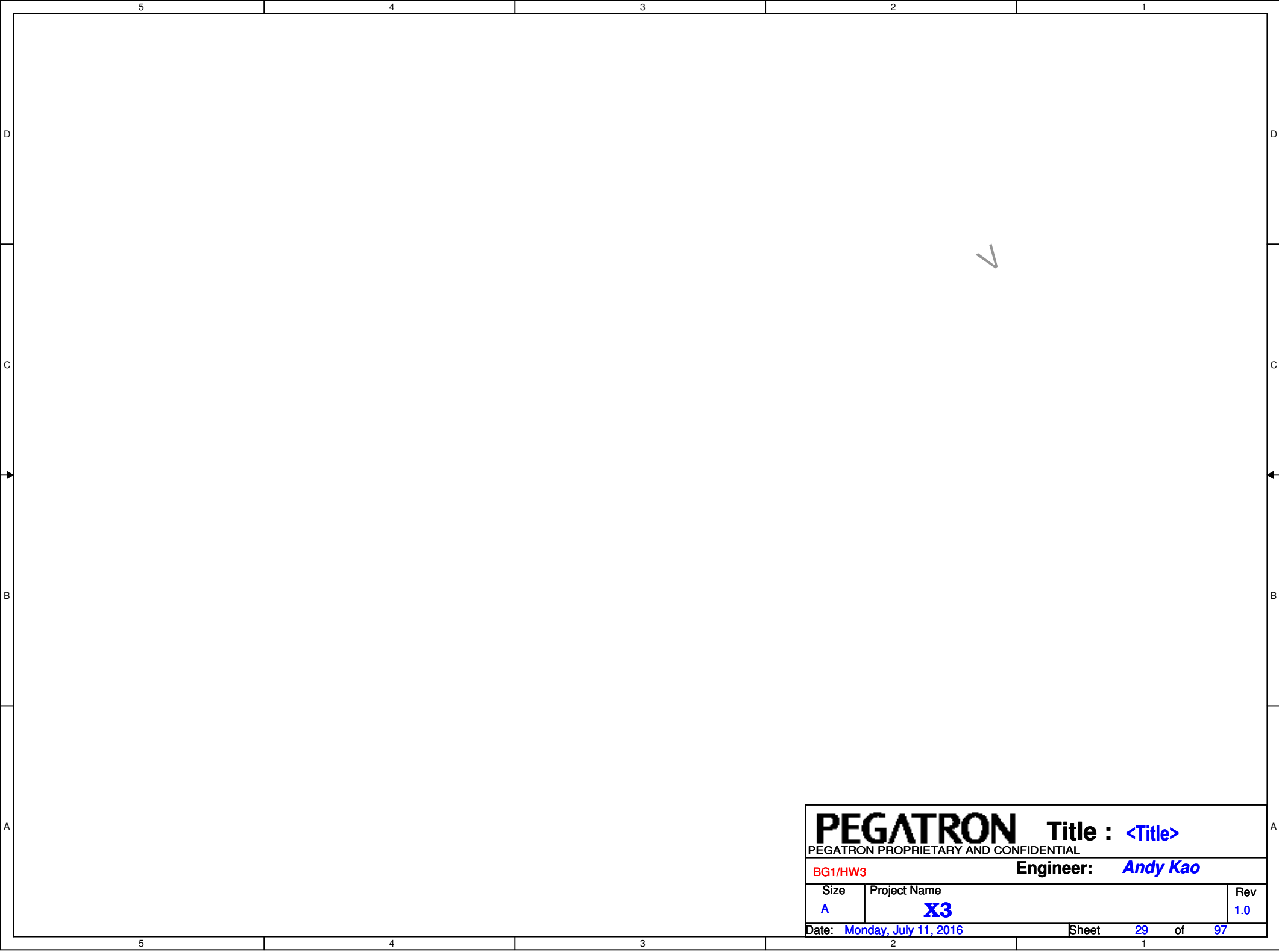
Icc (A)	Details
0.064	All HSI0 disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GBE Port
0.132	Each SATA Gen3 Port

SATA Gen3 Port X2
PCIe Gen2 Lane X1
USB3 Port X2
All HSI0 disabled (basic consumption)
=0.132x2+0.102+0.132x2+0.064 = 0.694A



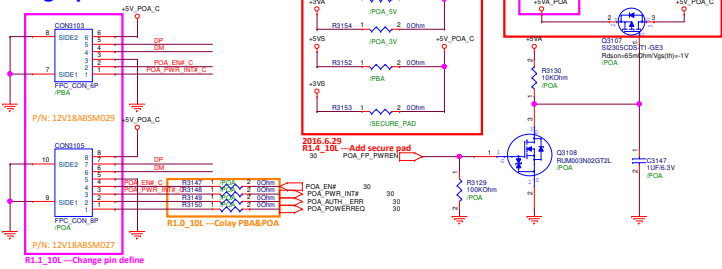


PEGATRON Title : <Title>		
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Size A	Project Name X3	Rev 1.0
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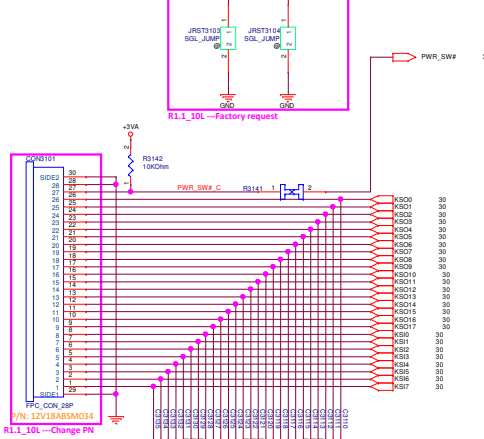


PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>29</i> of <i>97</i>

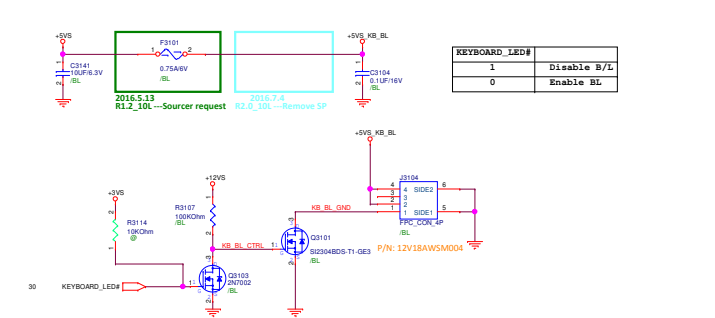
Fingerprinter



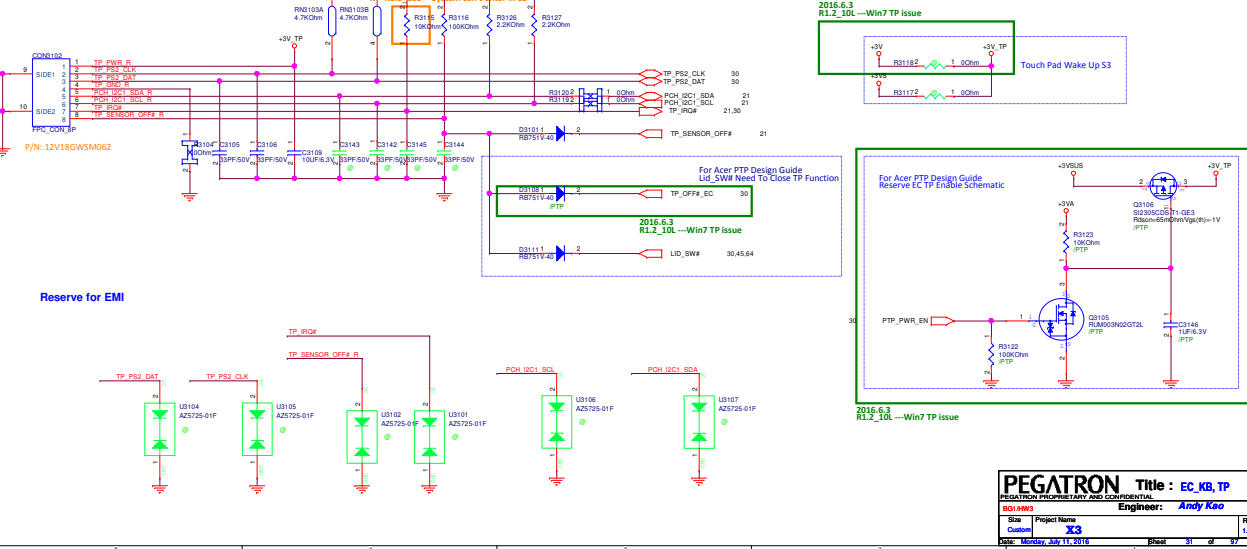
Keyboard

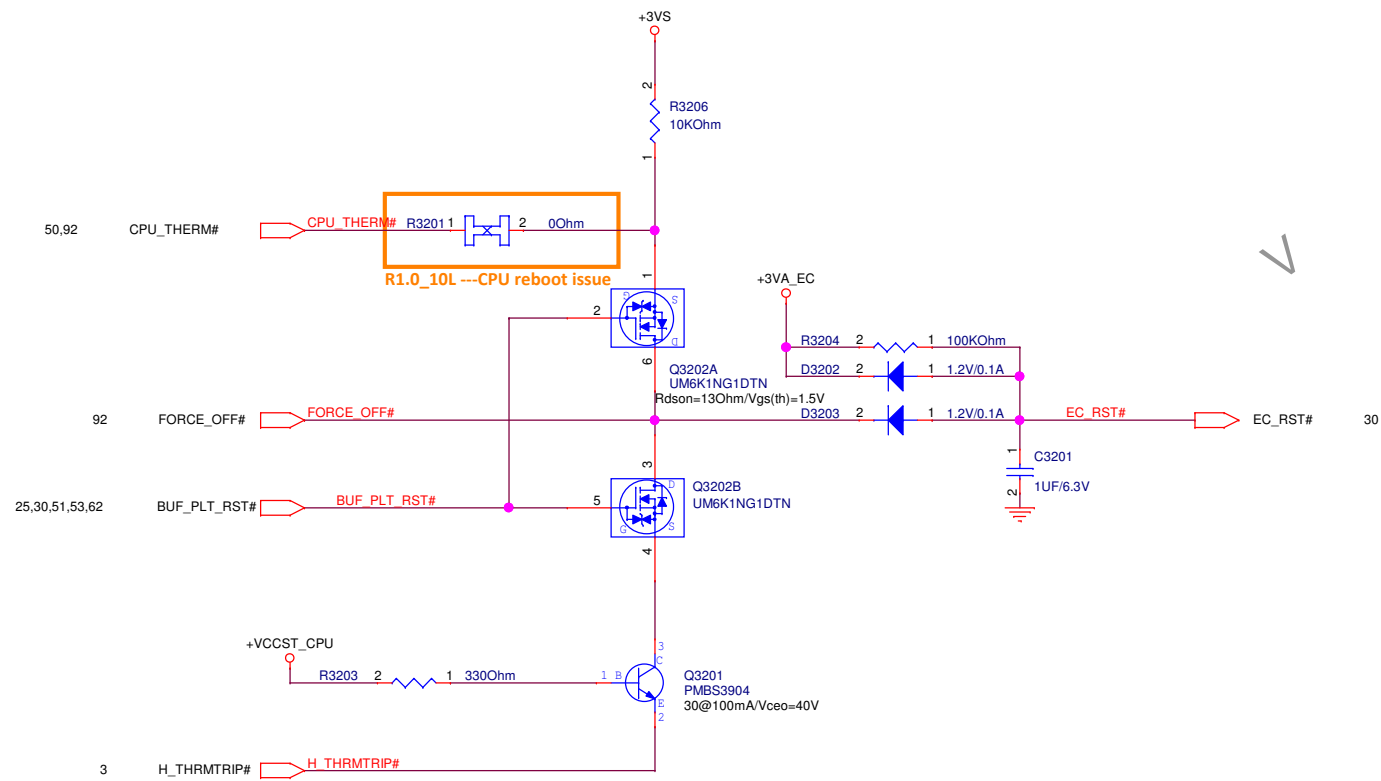


Keyboard LED

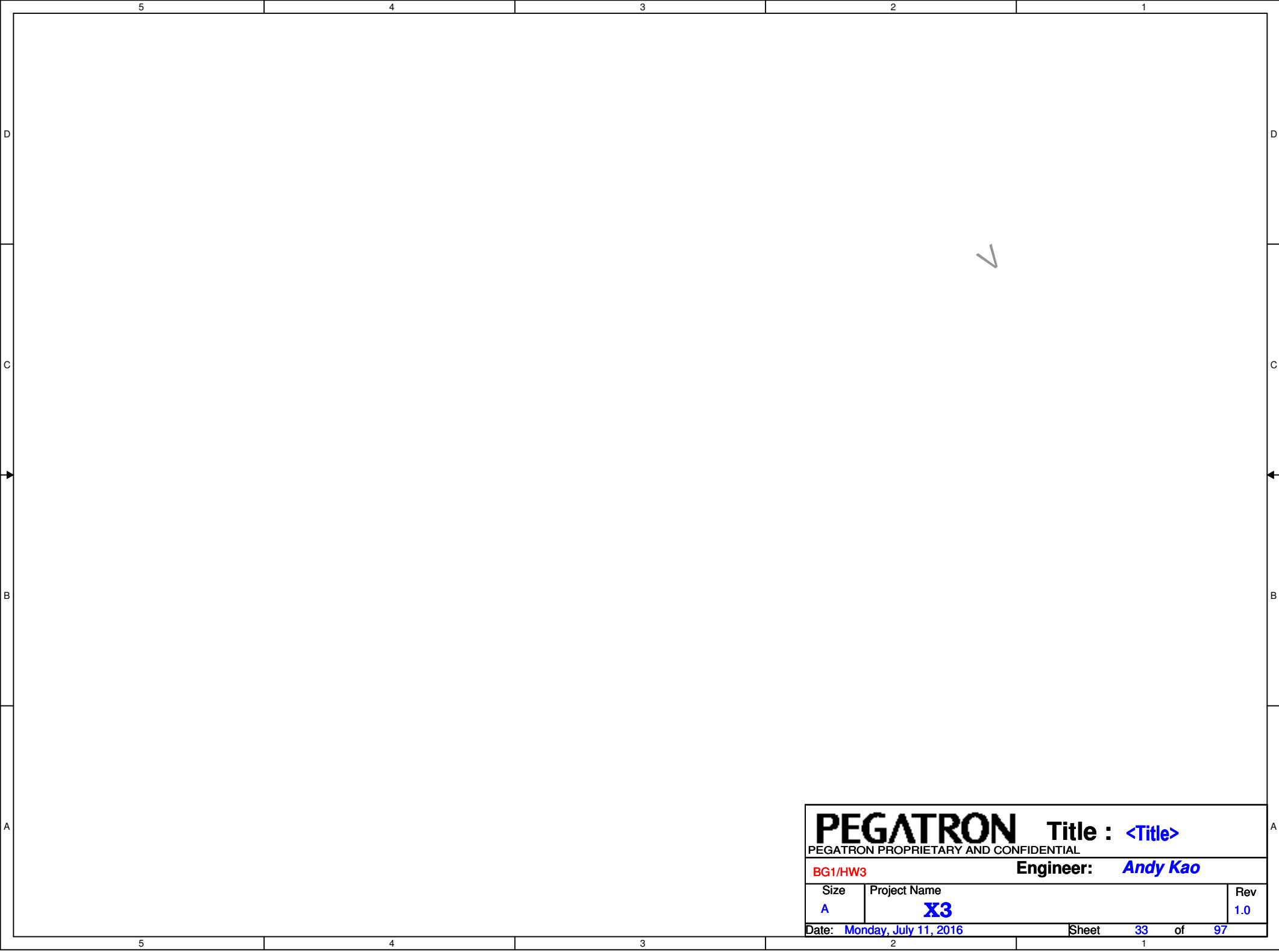


Click Pad

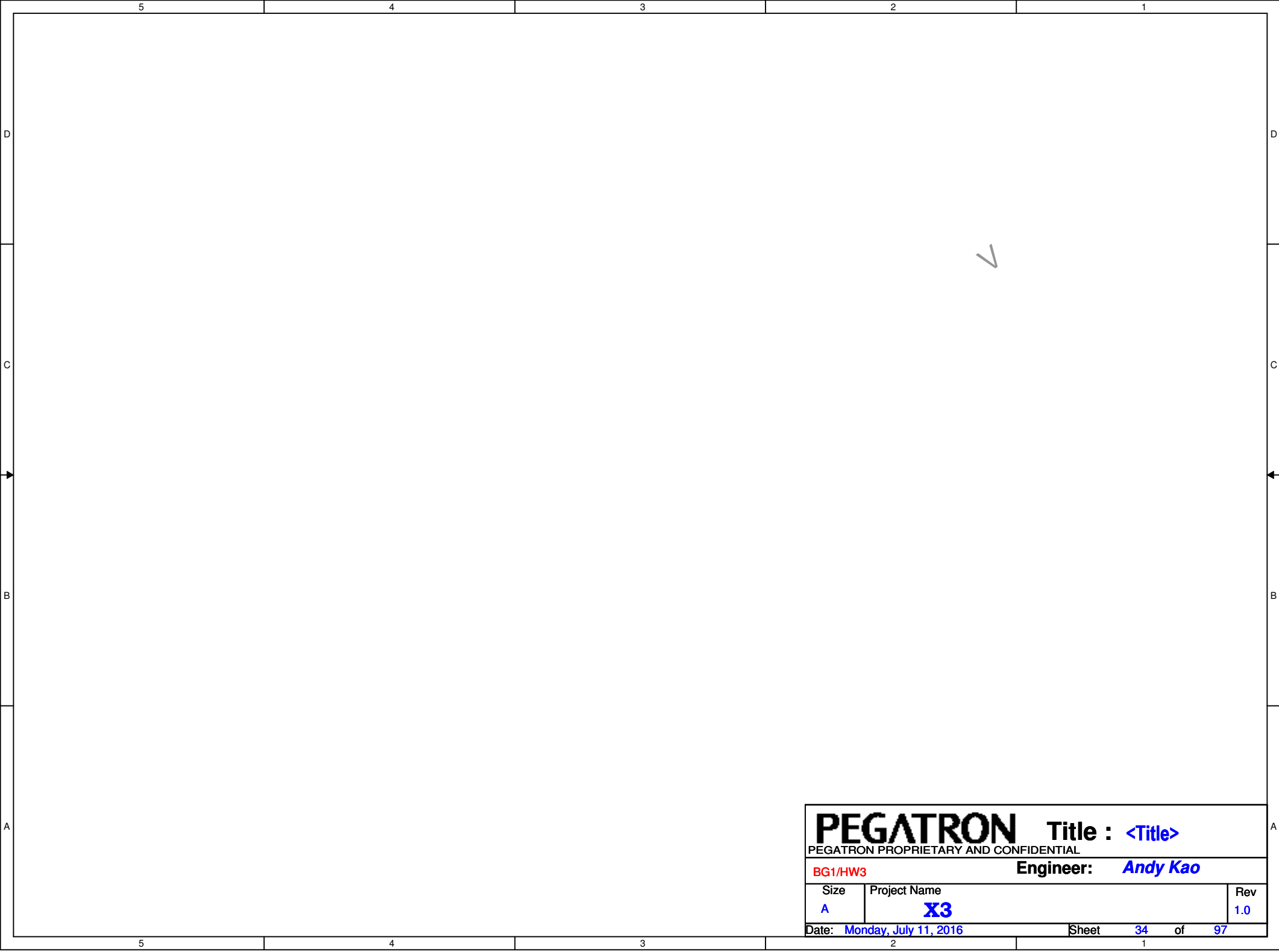




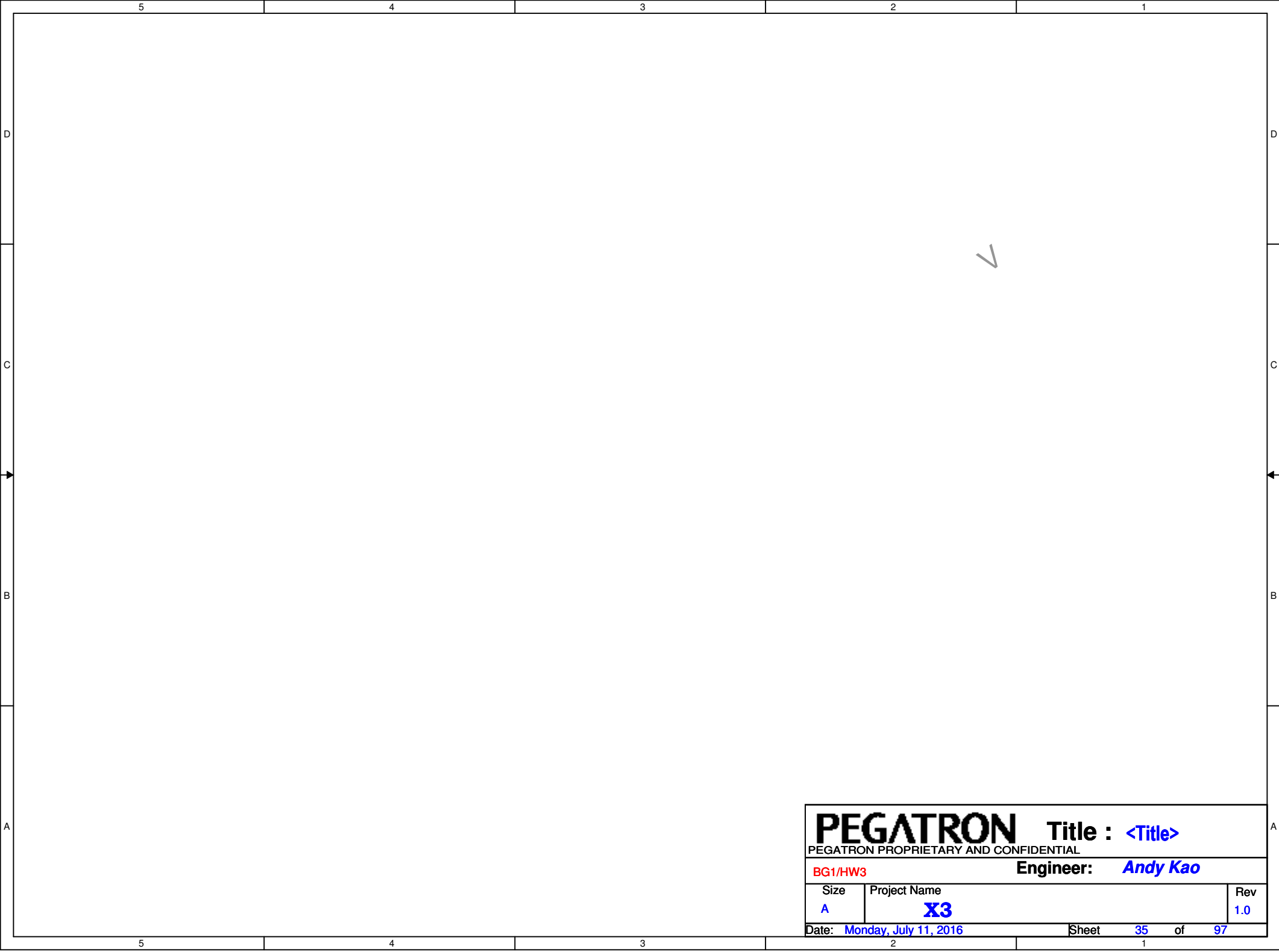
+VCCST_CPU → +VCCST_CPU 3,5,7,9,25
+3VA_EC → +3VA_EC 28,30,44
+3VS → +3VS 3,4,21,22,23,24,30,31,36,37,44,45,47,50,51,53,57,62,64,91,92



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PEGATRON Title : <Title>		
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Size A	Project Name X3	Rev 1.0
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D

D

C

C

B

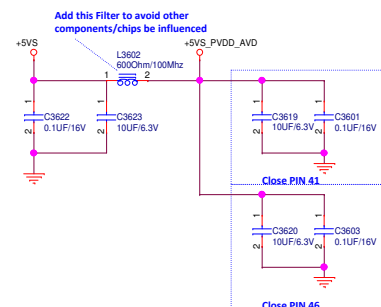
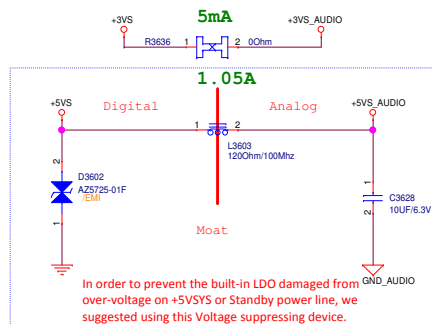
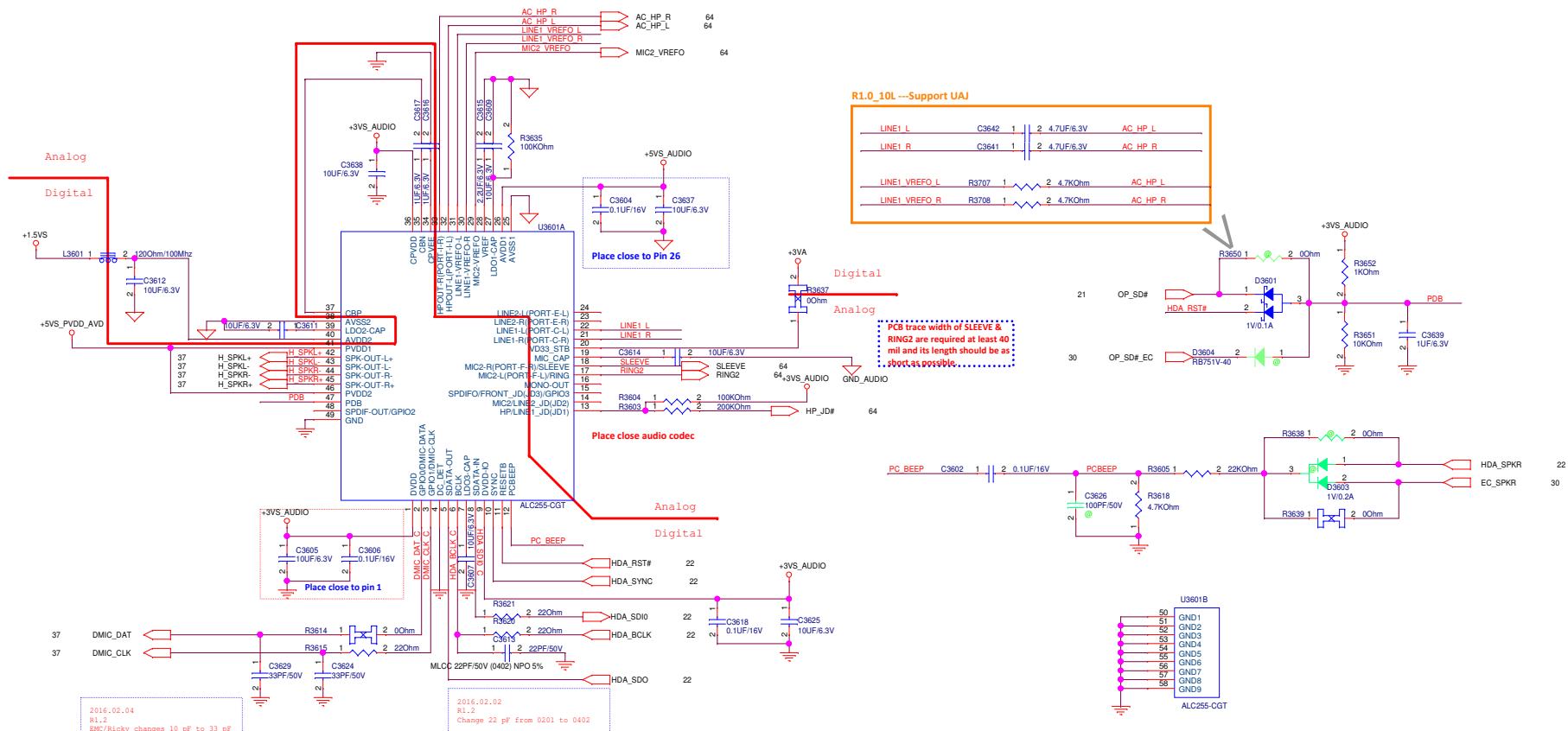
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A

A

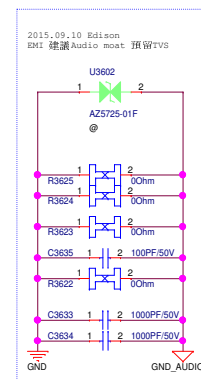
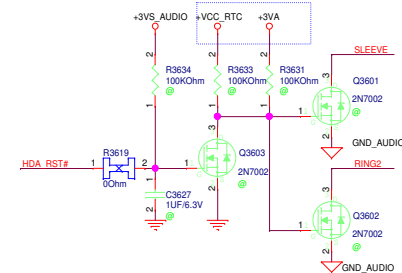
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BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
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+1.5VS	47.57.85
+3VS	3,4,21,22,23,24,30,31,32,37,44,45,47,50,51,53,57,62,64,91,92
+5VS	31,45,48,50,51,57,80,91

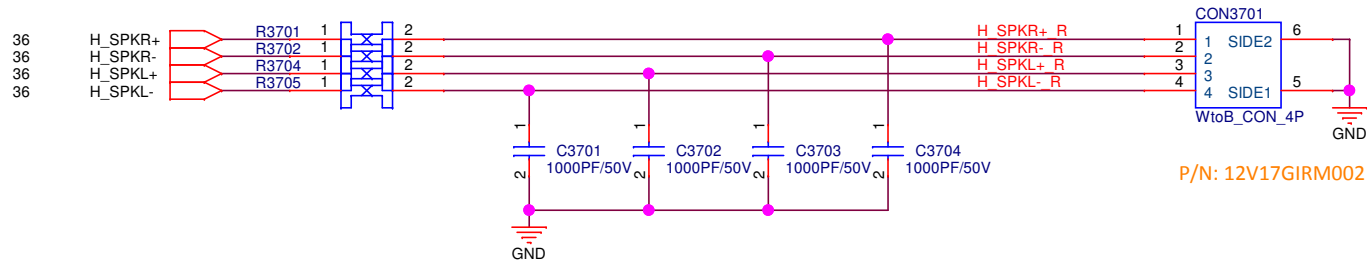


<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on, please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

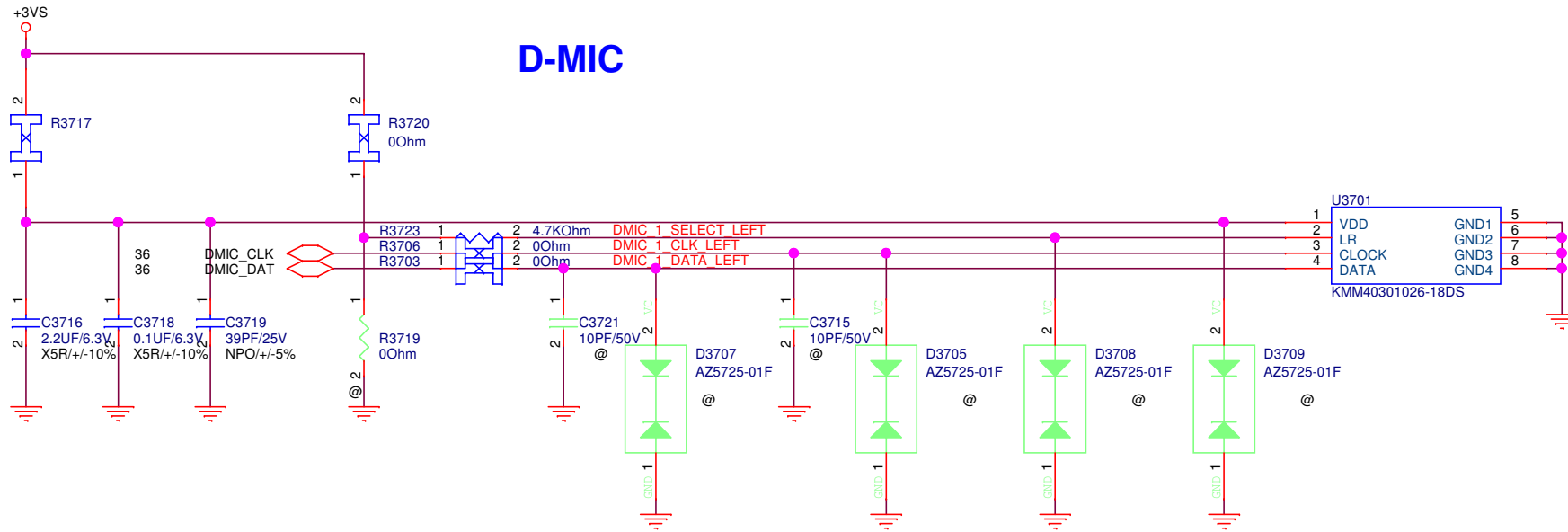
Grounding circuit for combo jack SLEEVE pin

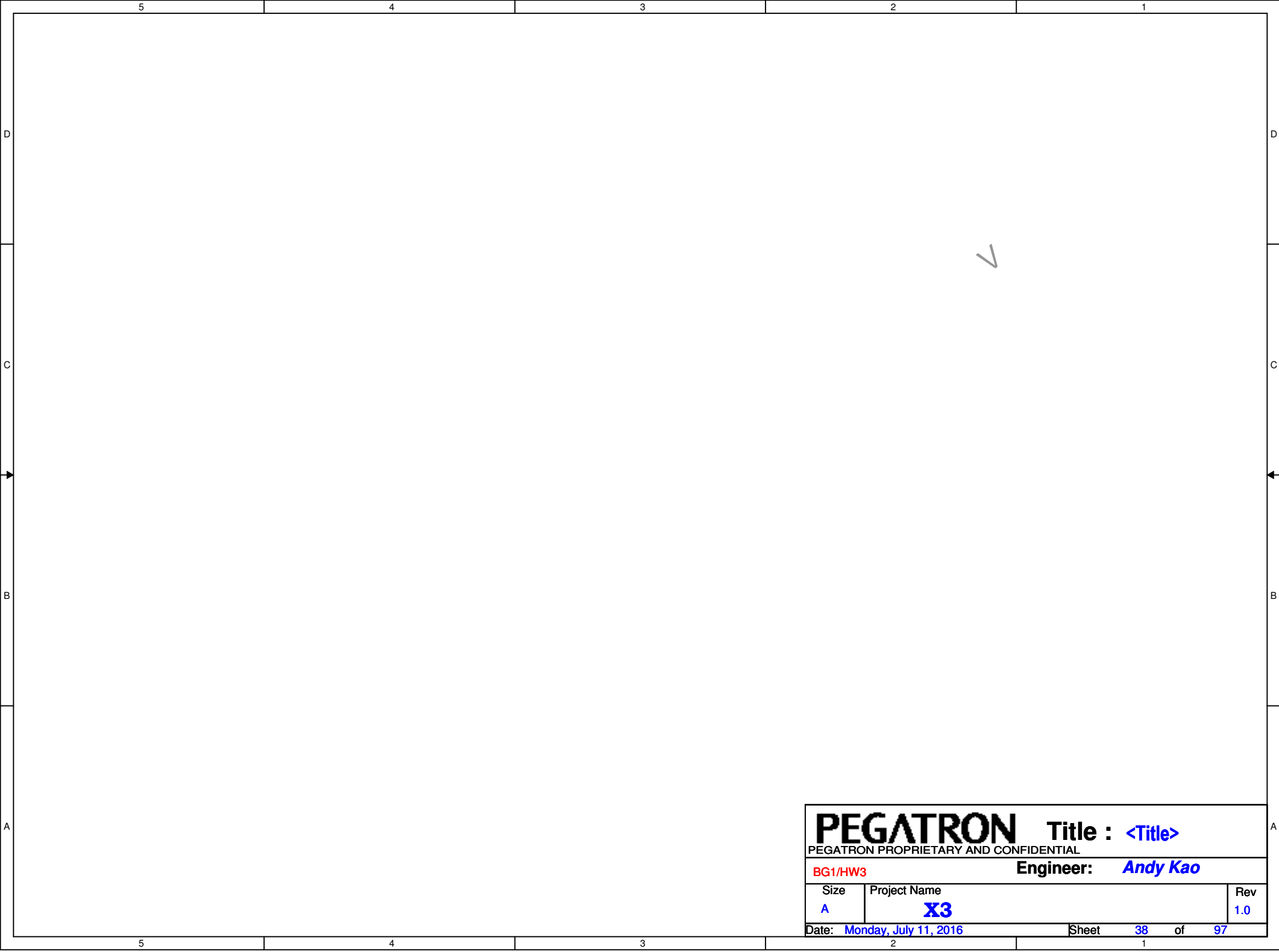


Speaker

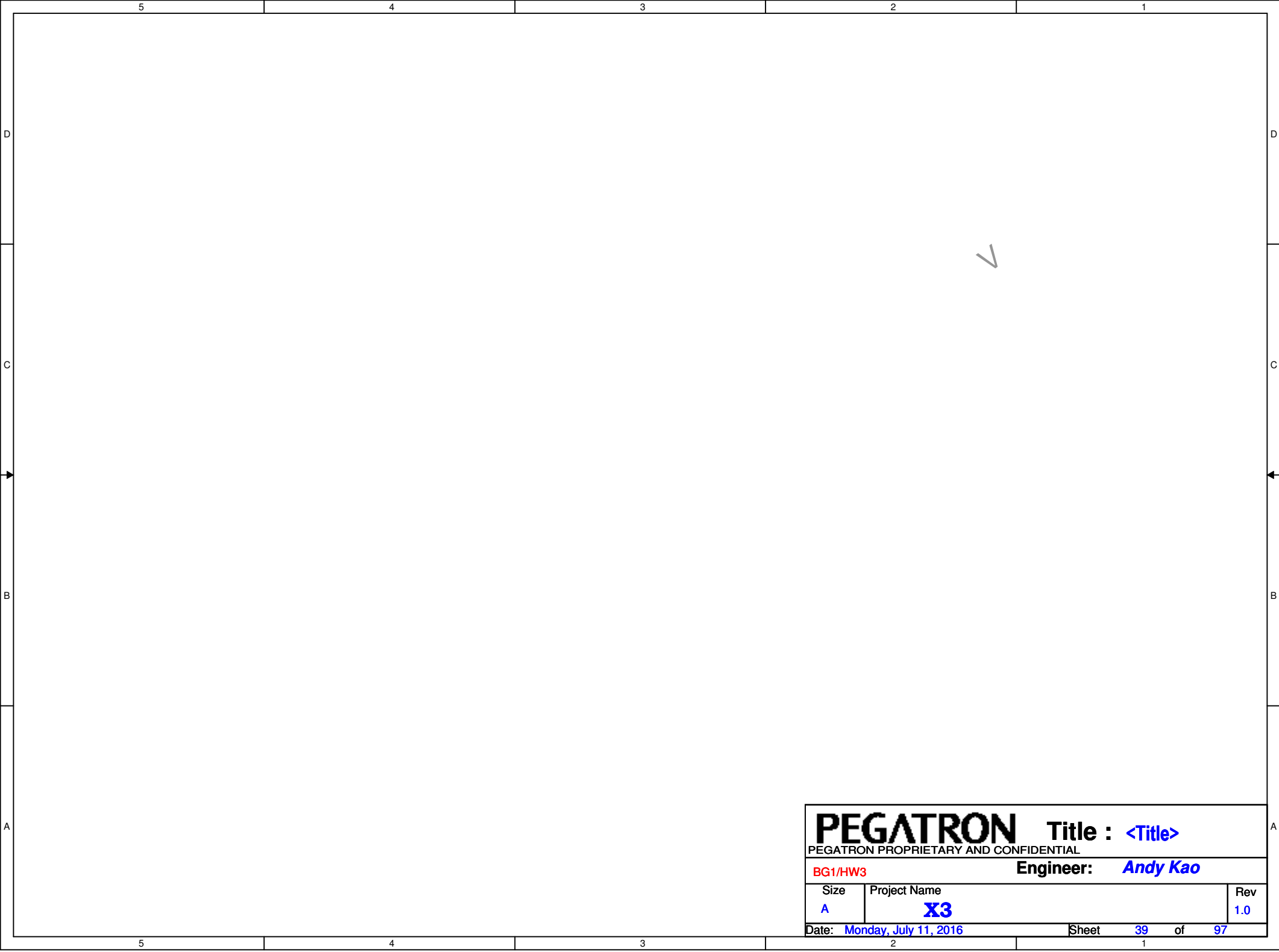


D-MIC





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BG1/HW3		Engineer: <i>Andy Kao</i>	
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D

D

C

C

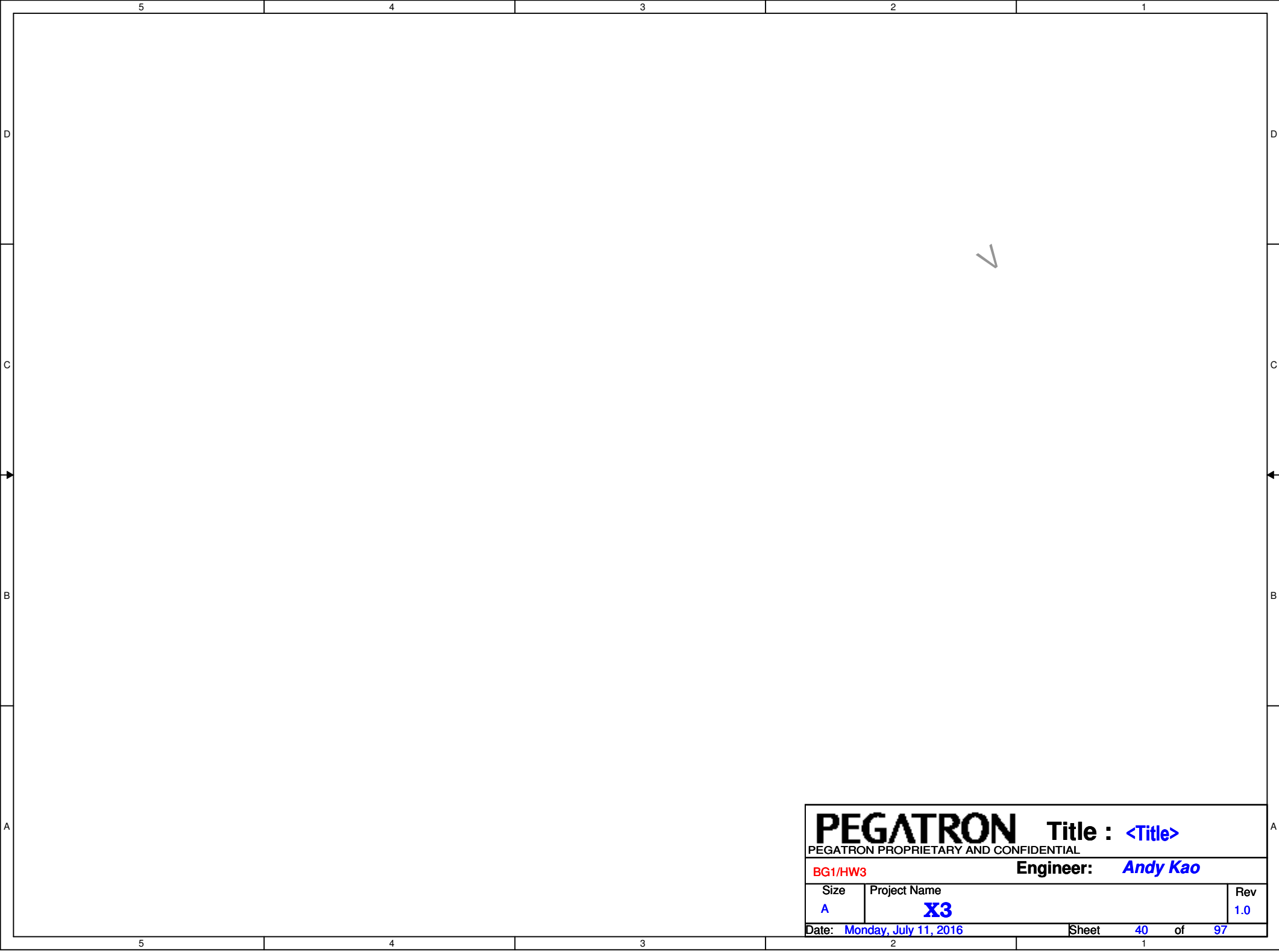
B

B

A

A

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BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
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D

D

C

C

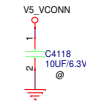
B

B

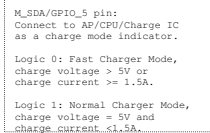
A

A

PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size A	Project Name X3	Rev 1.0
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The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.



I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD

1. Don't care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.

CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

Note:

1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse in DRP mode when cable is unplugged in ES chip.
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.

INTP_OUT pin: interrupt output.
Connect to AP or CPU.

```

triggered, set R16 = 4.7K, leave R22
not installed;
else if is high level triggered, set
=4.7K, leave R16 not installed.

```

PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

I2C_ADR_1 and I2C_ADR_0 pins:

1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

PEGATRON Title : POWER_FLOWCHART
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Engineer: Andy Kao		
Size C	Project Name X3	Rev 1.0
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Hardware Solution For Dead Battery

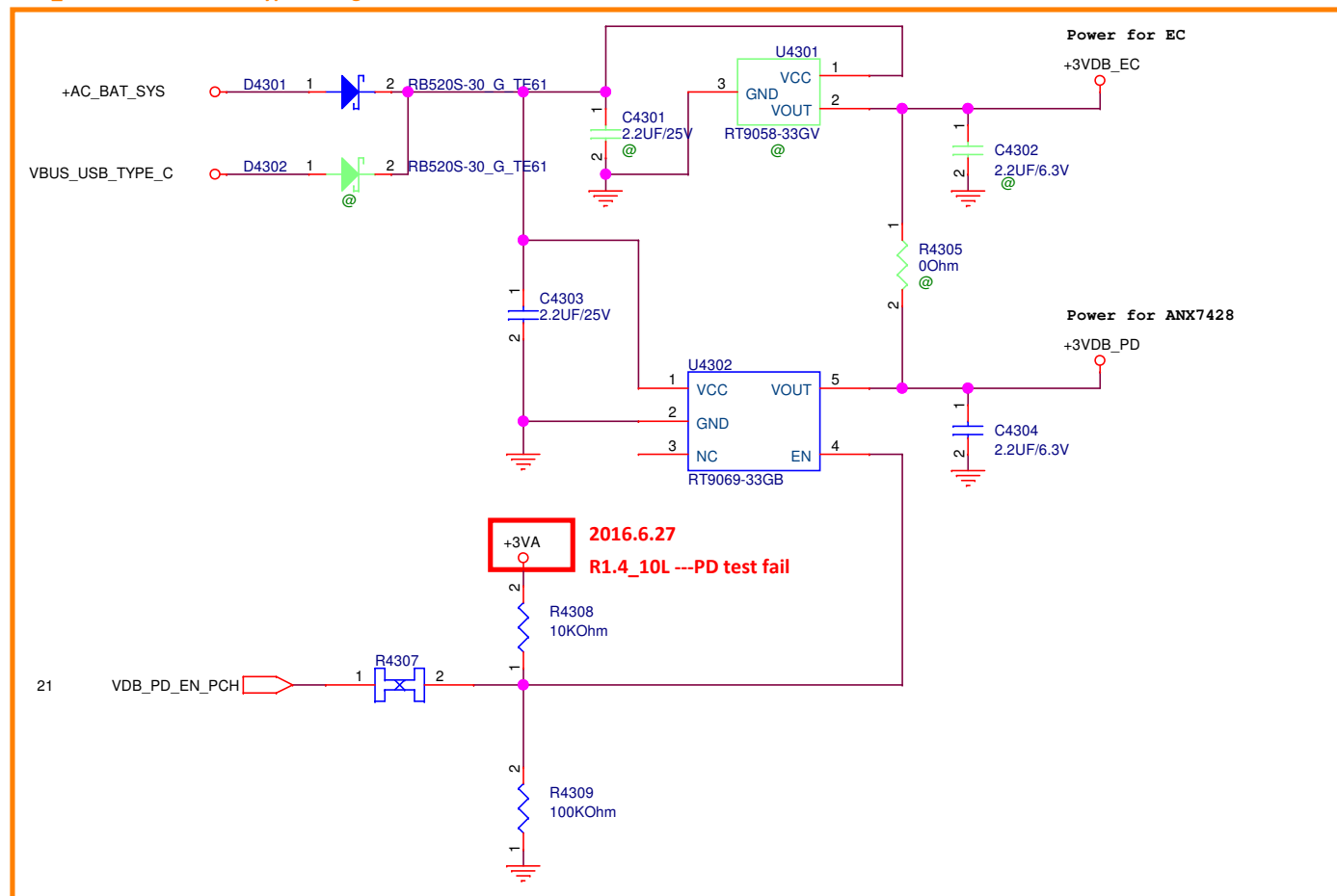
For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	41,42
+AC_BAT_SYS		+AC_BAT_SYS	45,80,81,82,83,88
+3VDB_EC		+3VDB_EC	30
+3VDB_PD		+3VDB_PD	41

Requirement of U1:

- 1) Vin range: 4V-30V.
- 2) Vout: EC's operating voltage + Vf of D1
- 3) Output current >= EC's operating current.

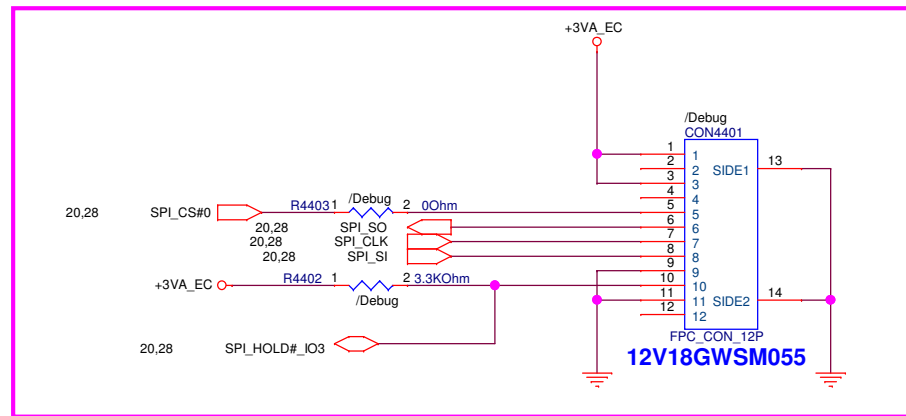
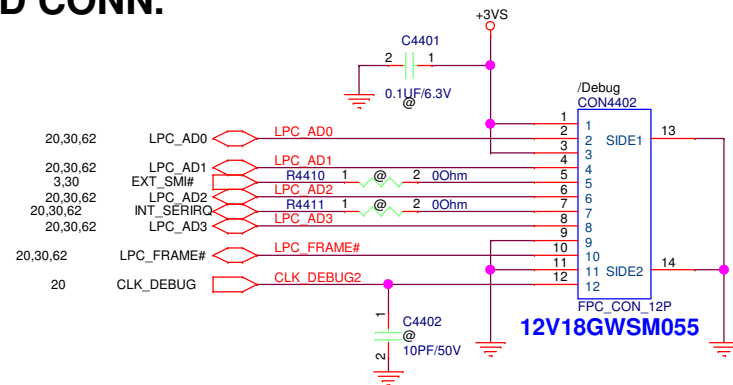
R1.0_10L ---Follow HAWAll type-c design



<Variant Name>

PEGATRON		Title : Dead Battery	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: Andy Kao			
Size Custom	Project Name X3	Rev 1.0	
Date:	Monday, July 11, 2016	Sheet	43 of 97

DEBUG CARD CONN.

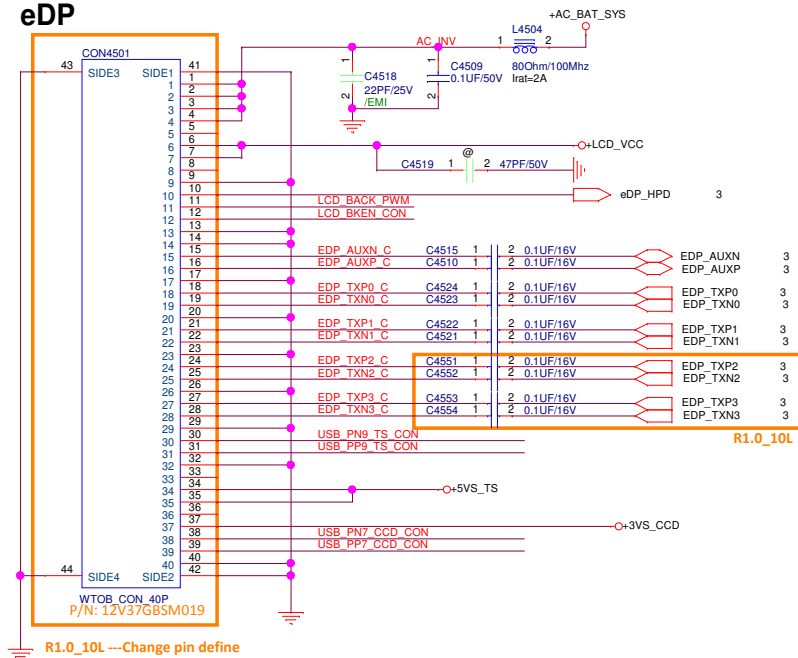


R1.1_10L ---BIOS request

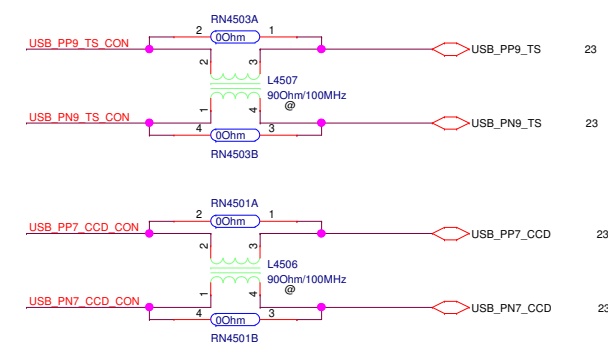
<Variant Name>

PEGATRON		Title : DEBUG CONN.	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 44 of 97	

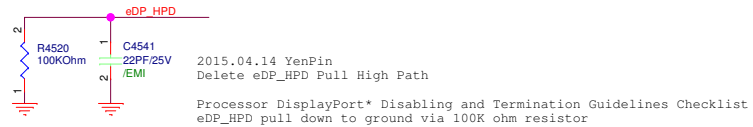
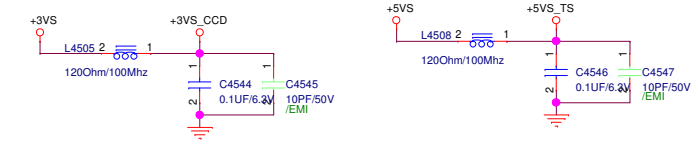
eDP



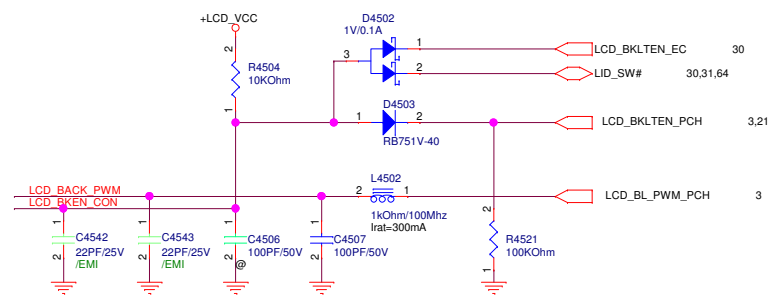
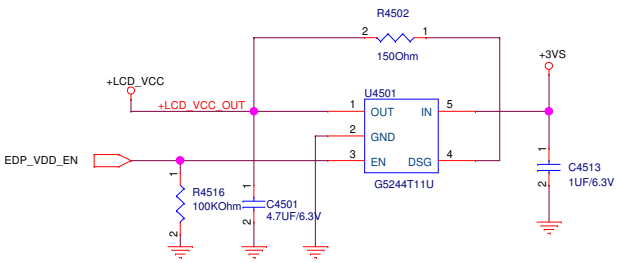
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,48,50,51,57,80,91
+AC_BAT_SYS	+AC_BAT_SYS	43,80,81,82,83,88



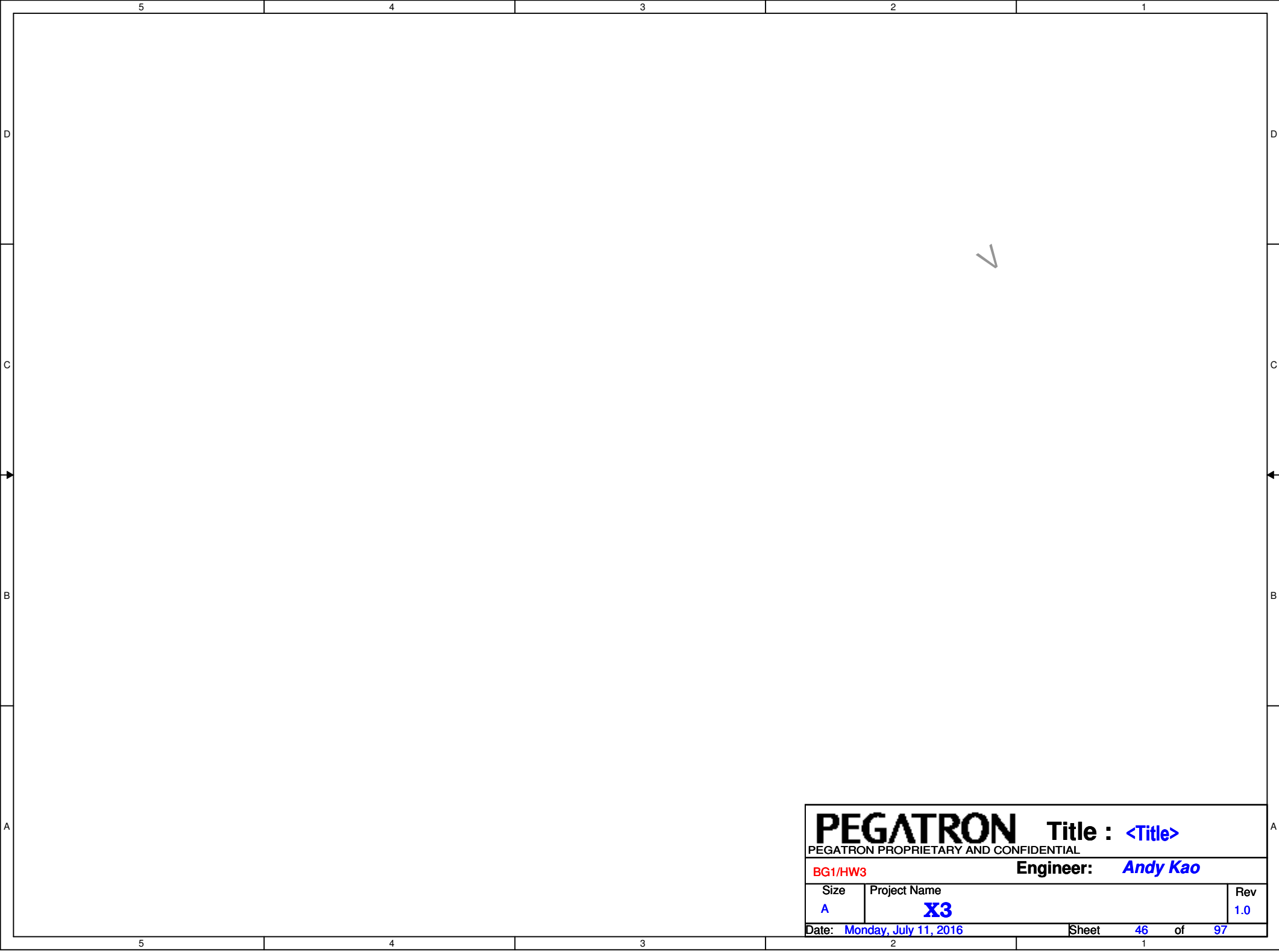
Camera



LCD VDDEN / +LED_VCC



<Variant Name>		Title : eDP CONN	
Size	Project Name	Engineer: Andy Kao	Rev
Custom	X3		1.0
Date: Monday, July 11, 2016	Sheet 45 of 97		



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<div><div>PEGATRON</div><div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div></div>			Title : <Title>		
BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
Date: Monday, July 11, 2016			Sheet	46	of 97

T4702 1 PRE

Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

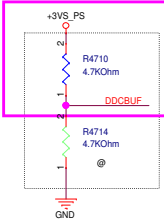
T4701 1 EQ

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.6dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

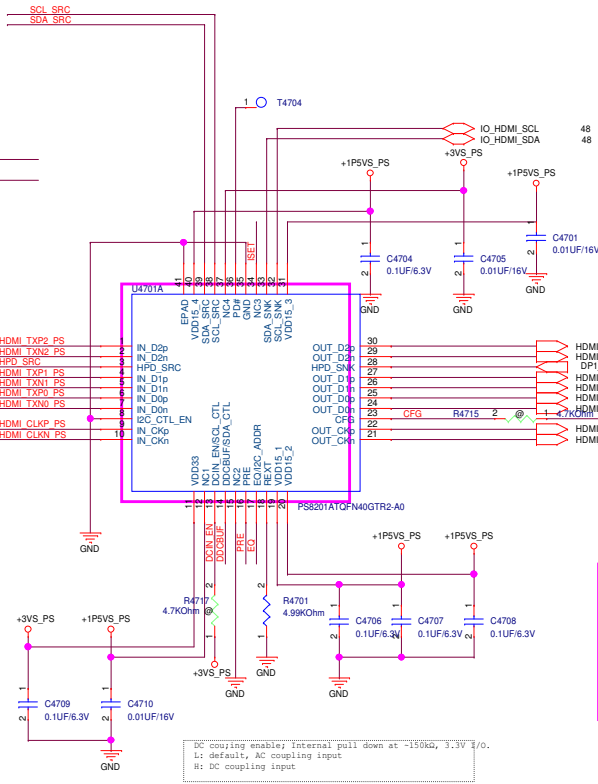
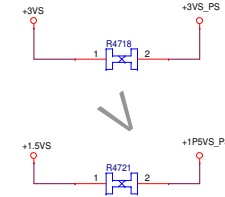
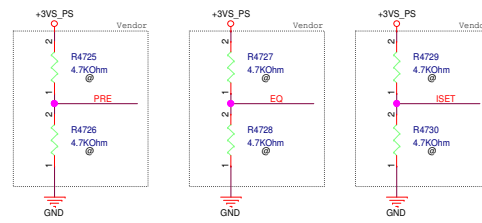
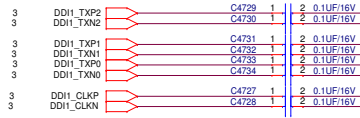
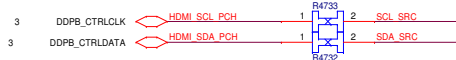
T4703 1 ISET

TMDS output swing adjustment; Internal pull down at ~150k, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

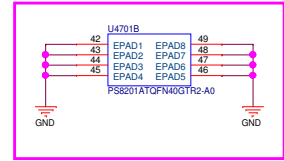
R1.1_10L ---Follow megatron



Enable active DDC buffer; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor



Configuration pin, 3.3V I/O, internal pull down at ~150k, 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable
(Typ:1.5V; Max:1.53V; Min:1.47V)

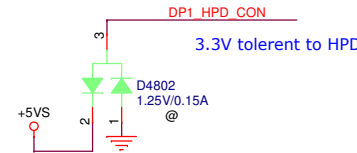
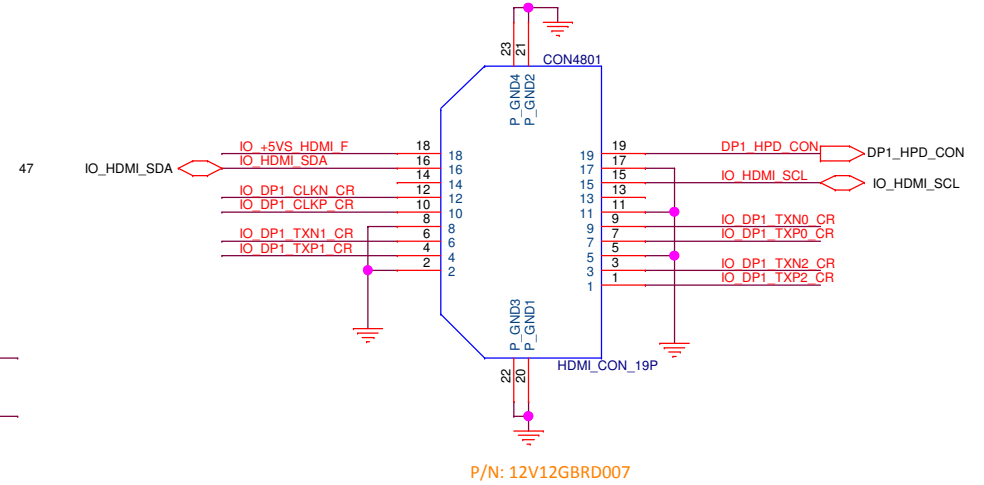
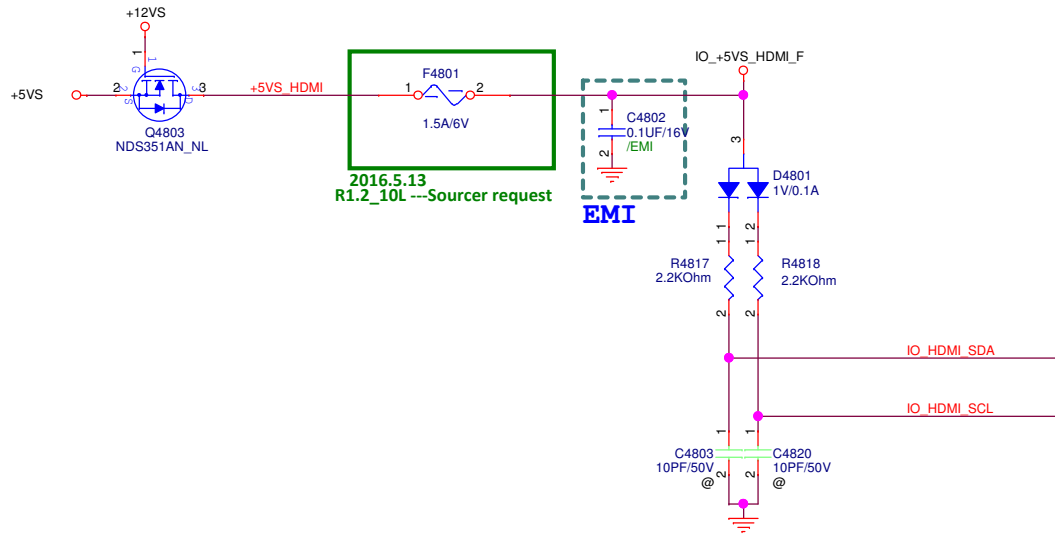


R1.1_10L ---Sourcer request

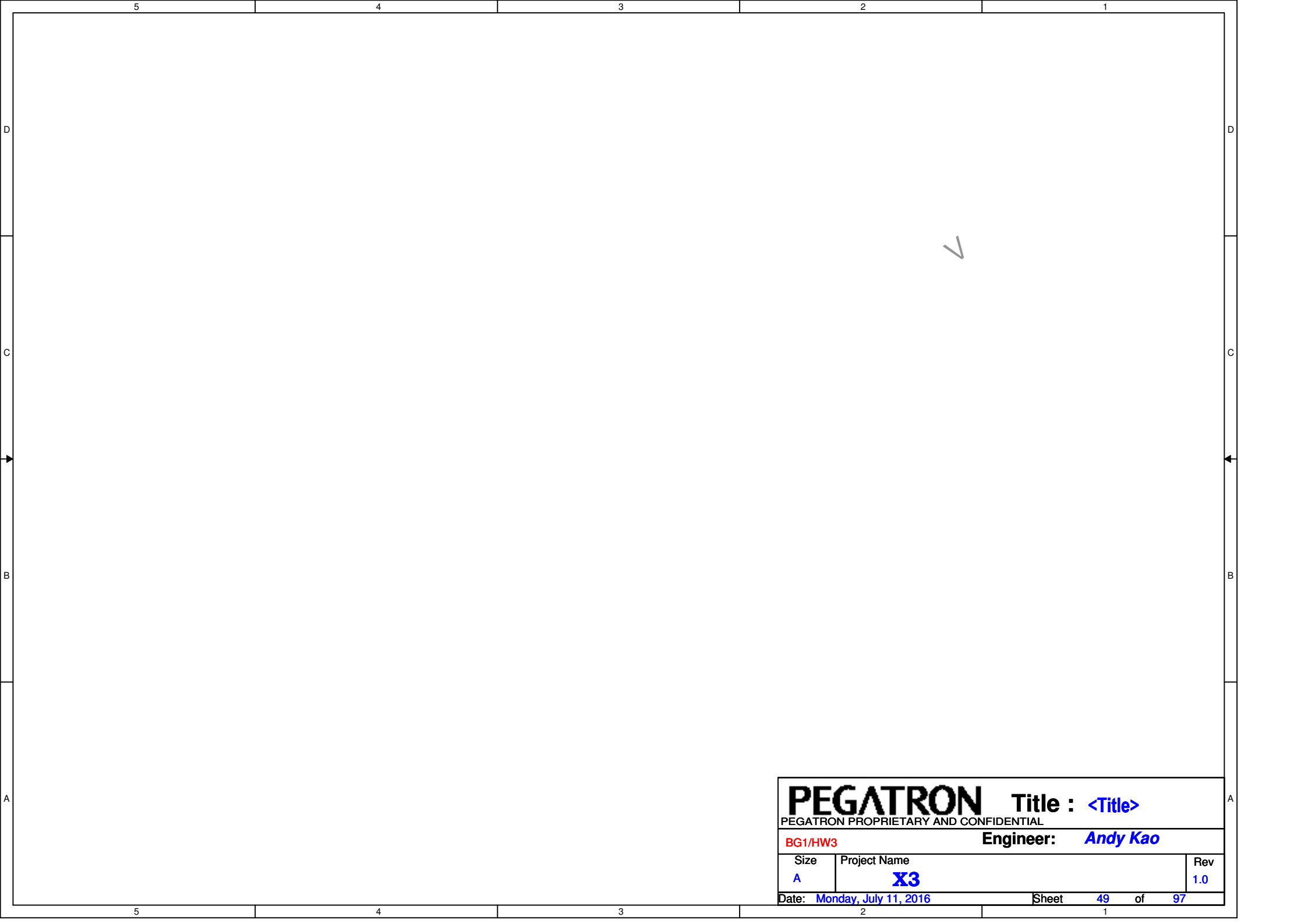
DC coupling enable; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

HDMI

+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,45,50,51,57,80,91
+12VS	+12VS	31,57,91



PEGATRON		Title : HDMI-4K2K	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
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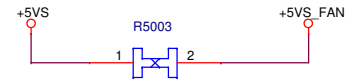
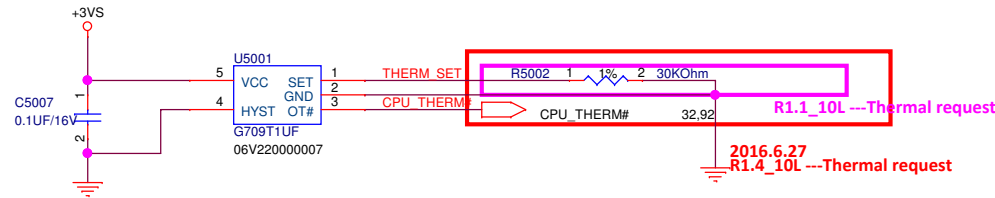


PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>49</i> of <i>97</i>

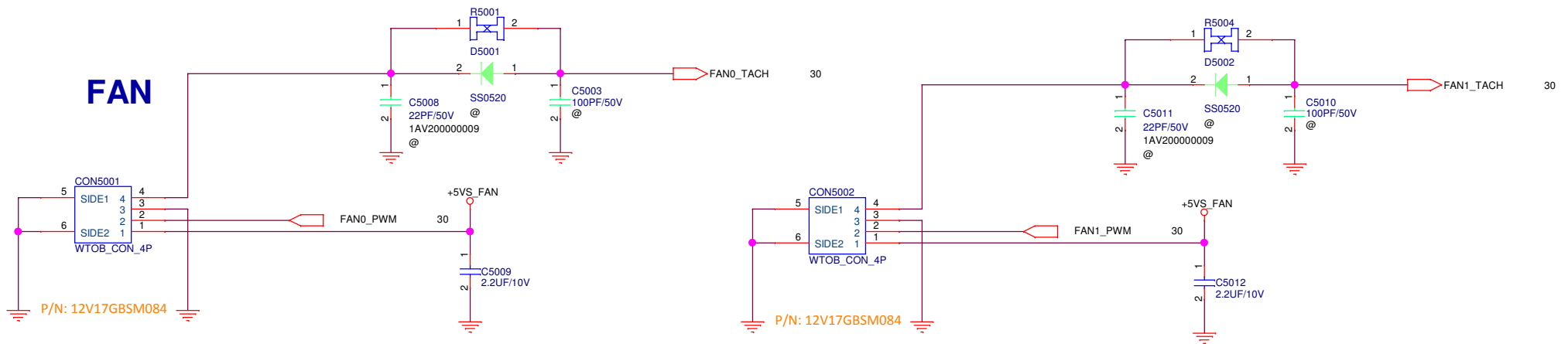
Thermal Sensor

temp setting : 80 degree

$RSET(k\Omega) = 0.0012T^{\circ}C - 0.9308T + 96.147$



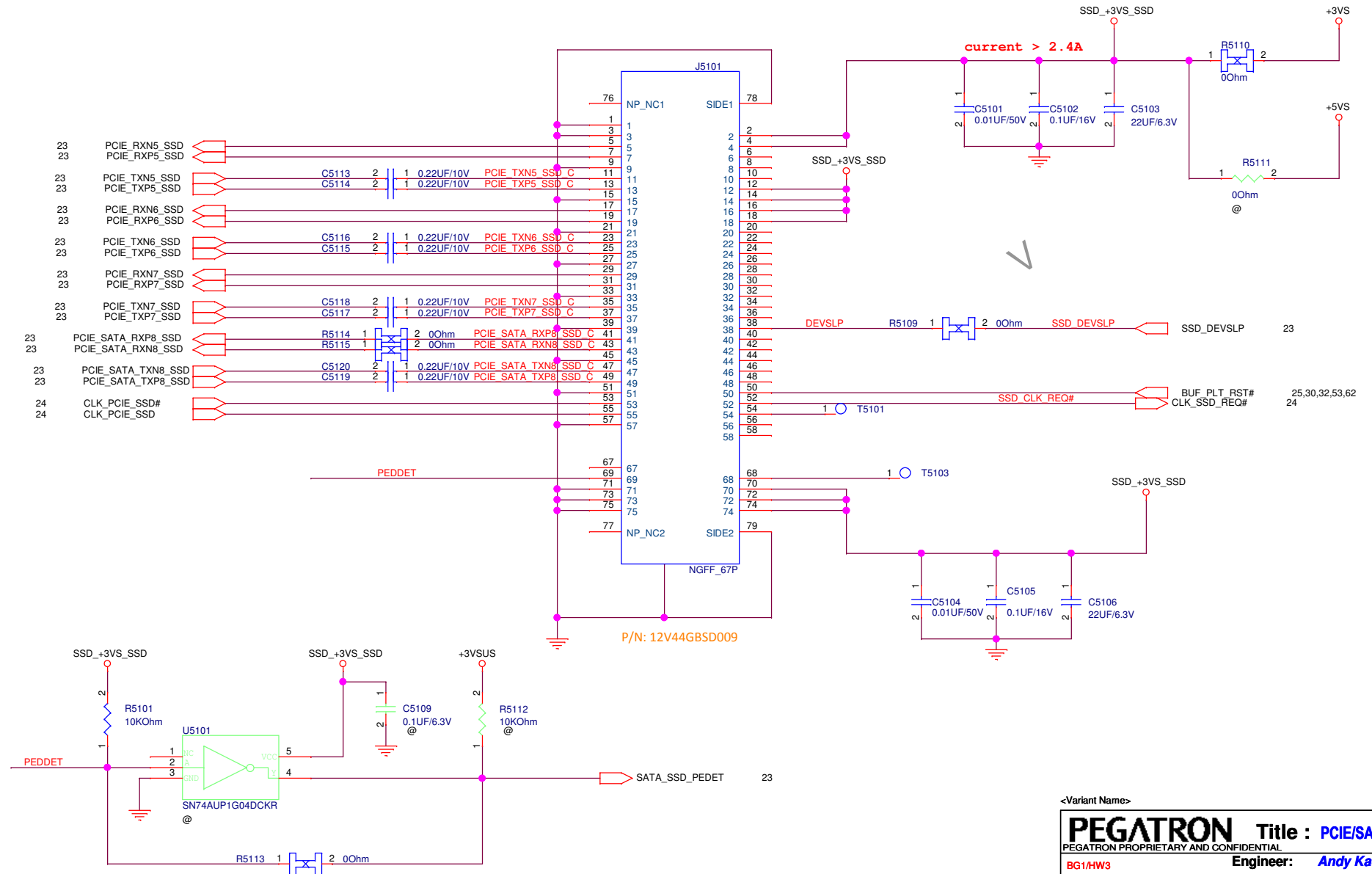
FAN



<Variant Name>

PEGATRON		Title : Thermal/Fan	
BG1/HW3		Engineer: Andy Kao	
Size	Project Name	Rev	
B	X3	1.0	
Date: Monday, July 11, 2016		Sheet 50 of 97	

SSD(SATA/PCIE x4) NGFF socket (M-key)



<Variant Name>

PEGATRON Title : **PCIe/SATA SSD**

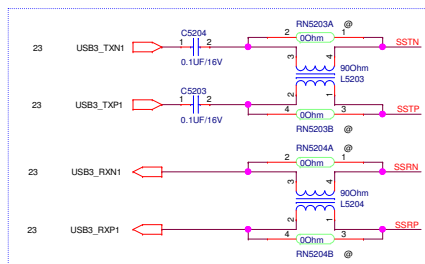
PEGATRON PROPRIETARY AND CONFIDENTIAL	
BG1/HW3	Engineer: <i>Andy Kao</i>

Size	Project Name	Rev
Custom	X3	1.0

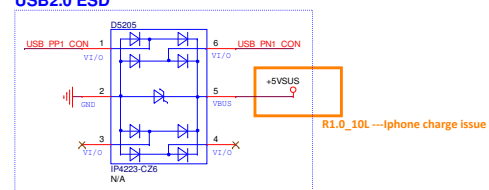
Date: Monday, July 11, 2016 Sheet 51 of 97

USB 3.0

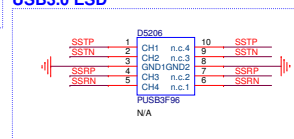
USB3.0 Choke



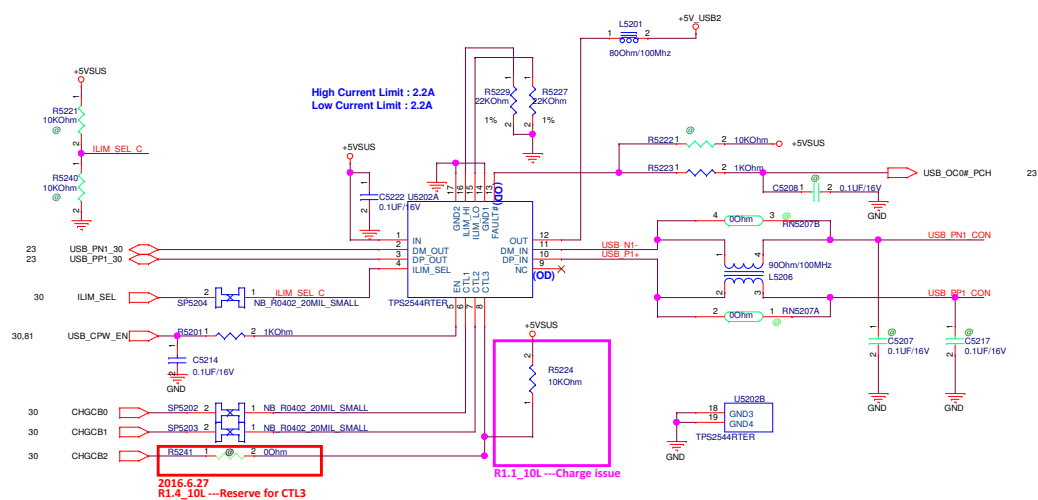
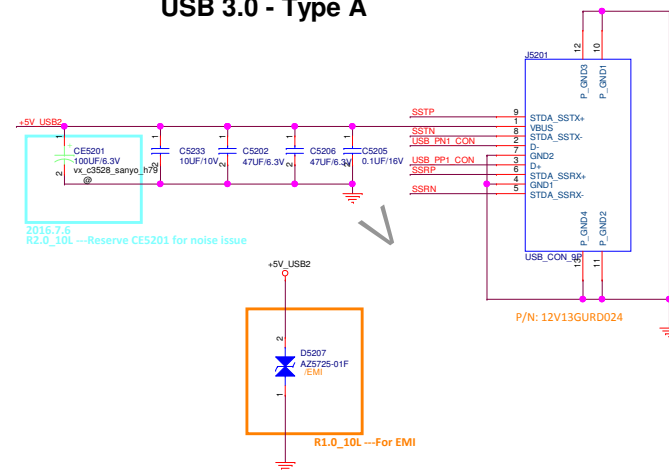
USB2.0 ESD



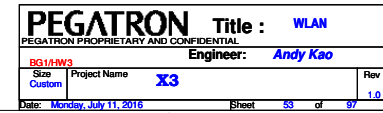
USB3.0 ESD

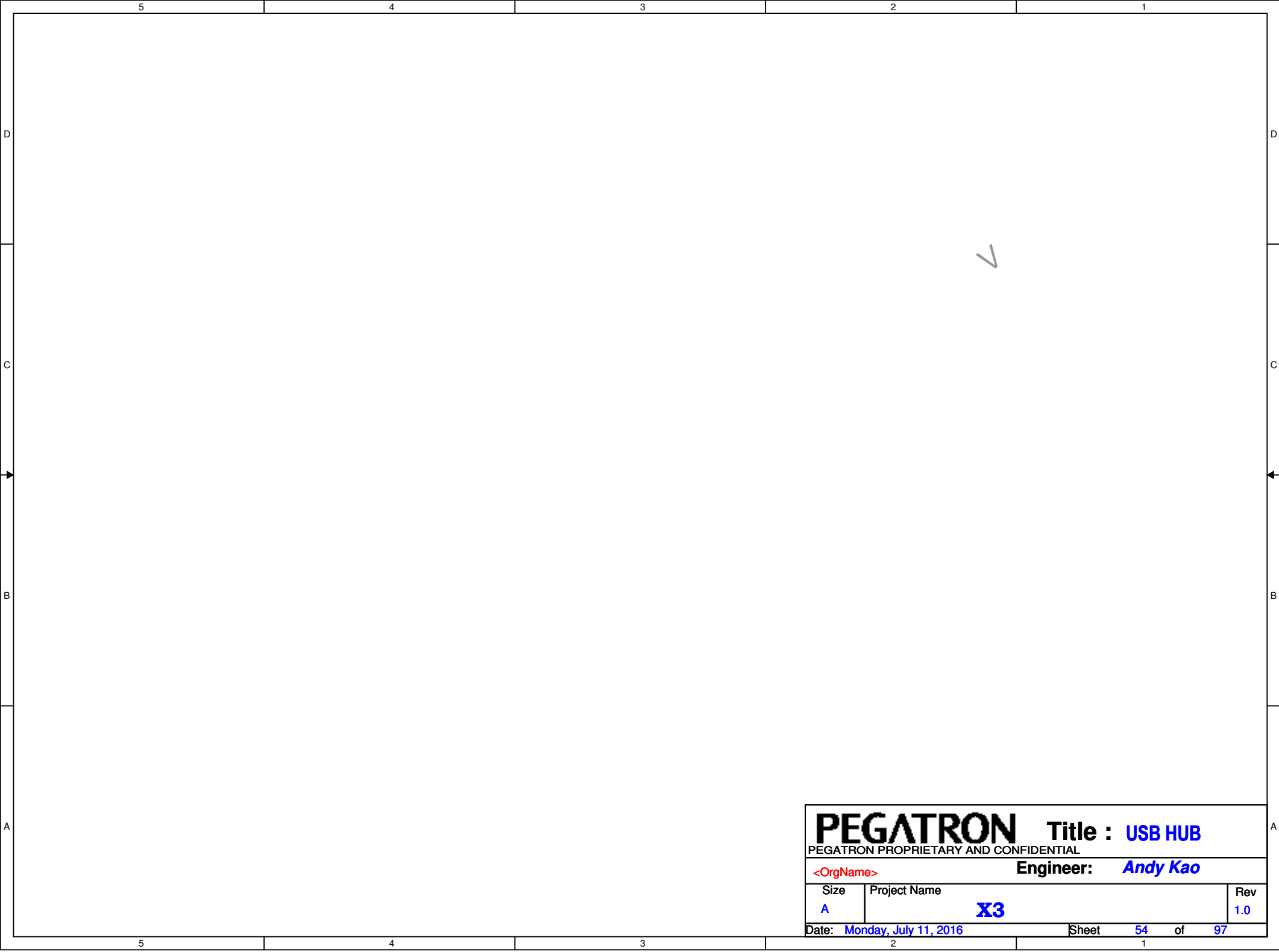


USB 3.0 - Type A



+3VS +3VS 3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,57,62,64,91,92





PEGATRON

Title : USB HUB

PEGATRON PROPRIETARY AND CONFIDENTIAL

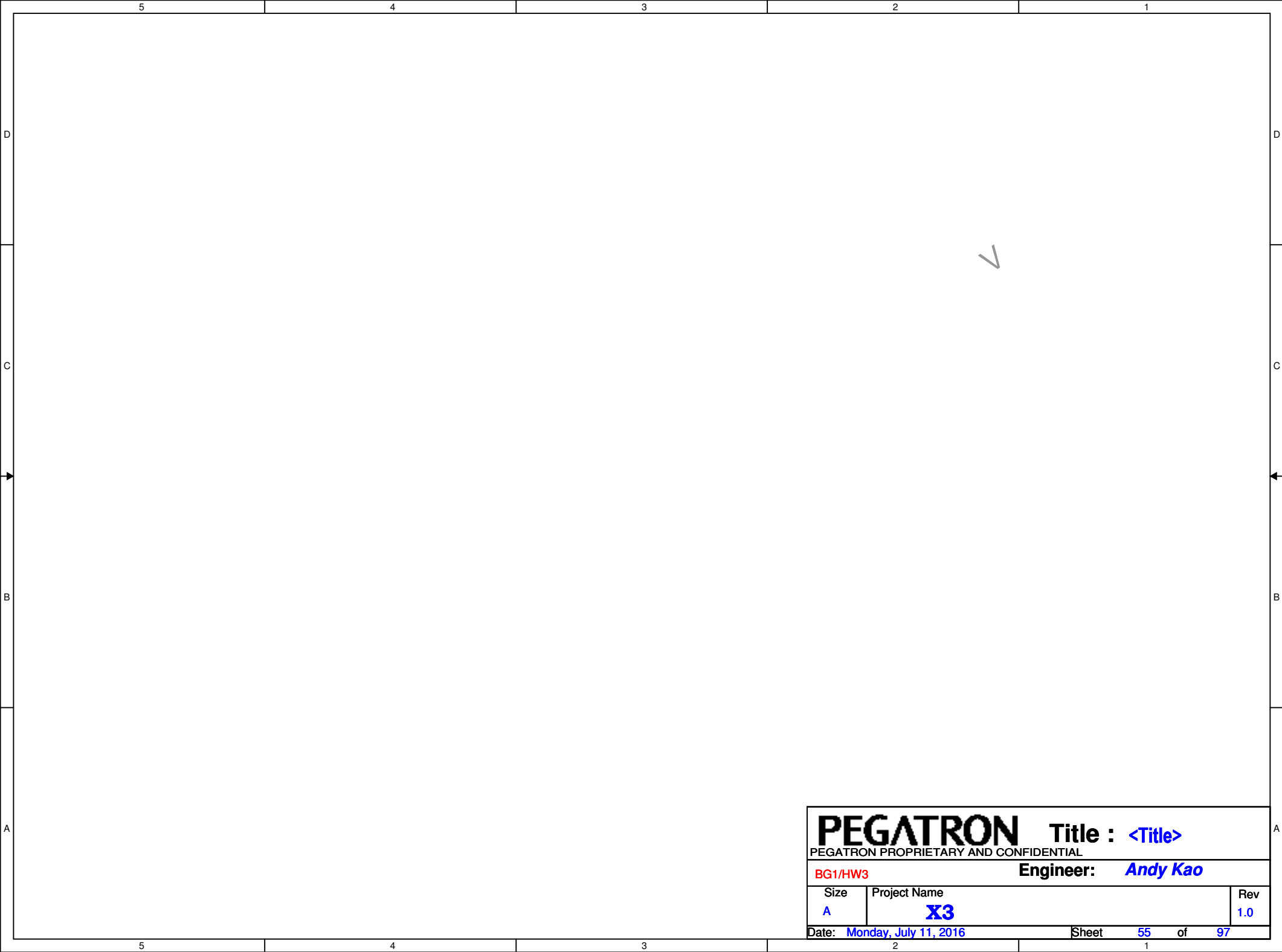
<OrgName>

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016

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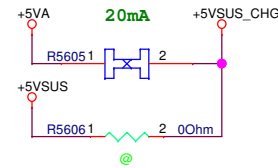
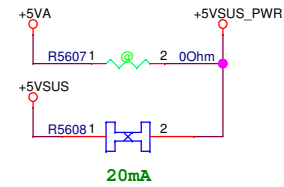
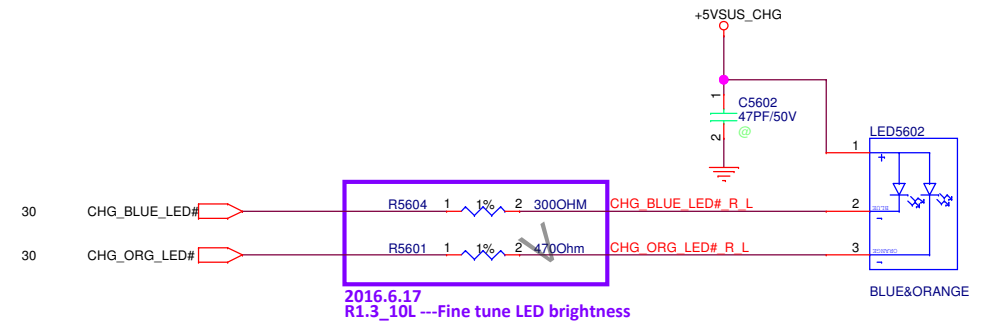
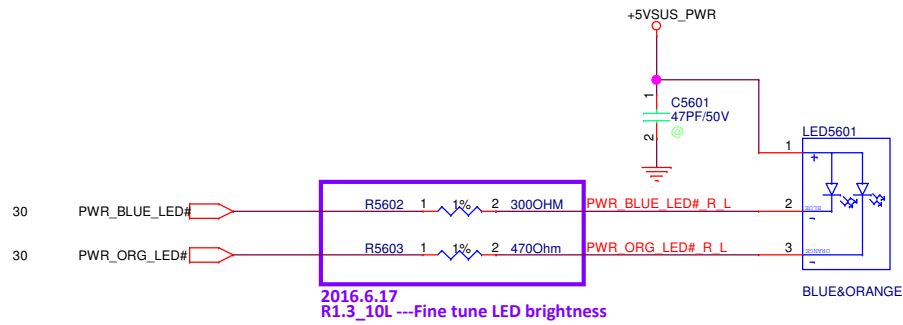
A

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PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 55 of 97

POWER LED

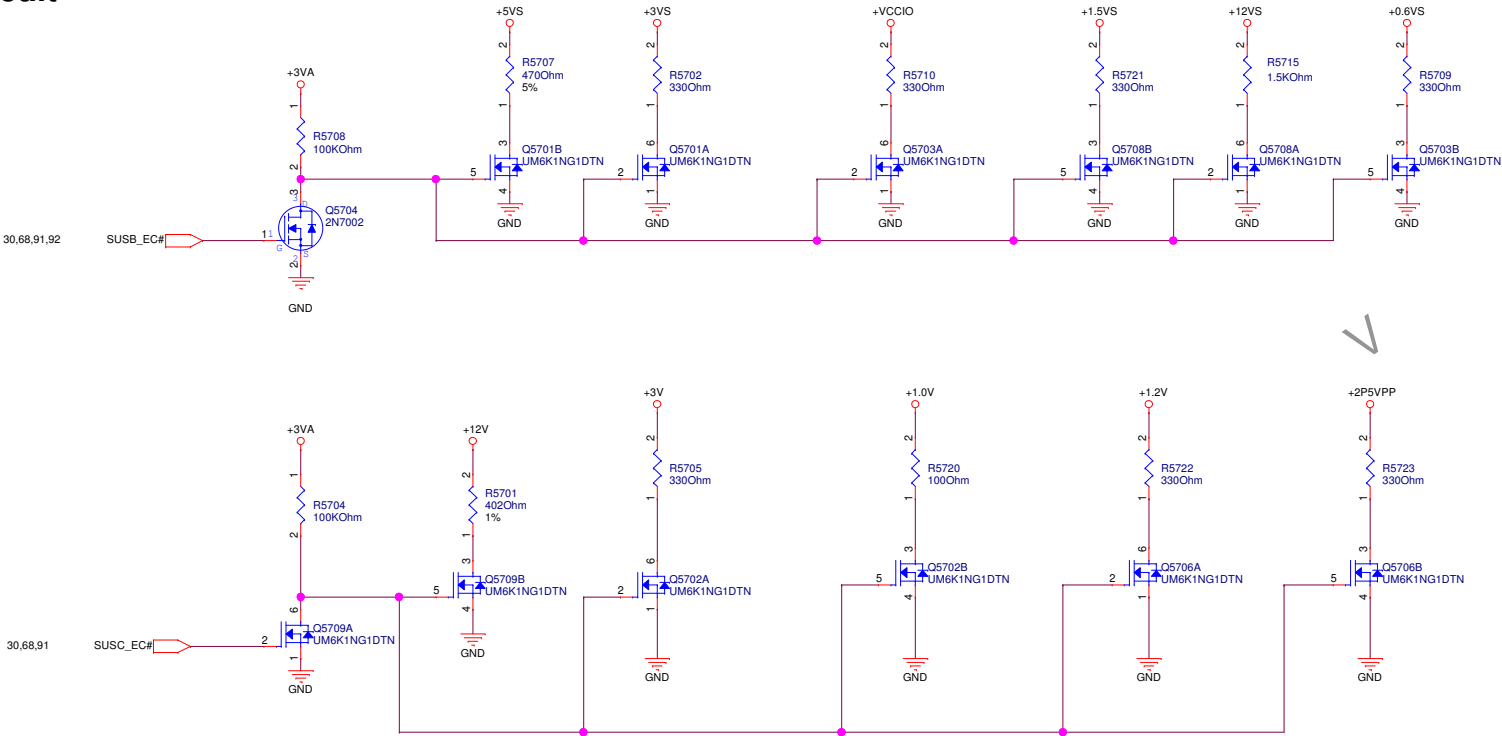
Charger LED

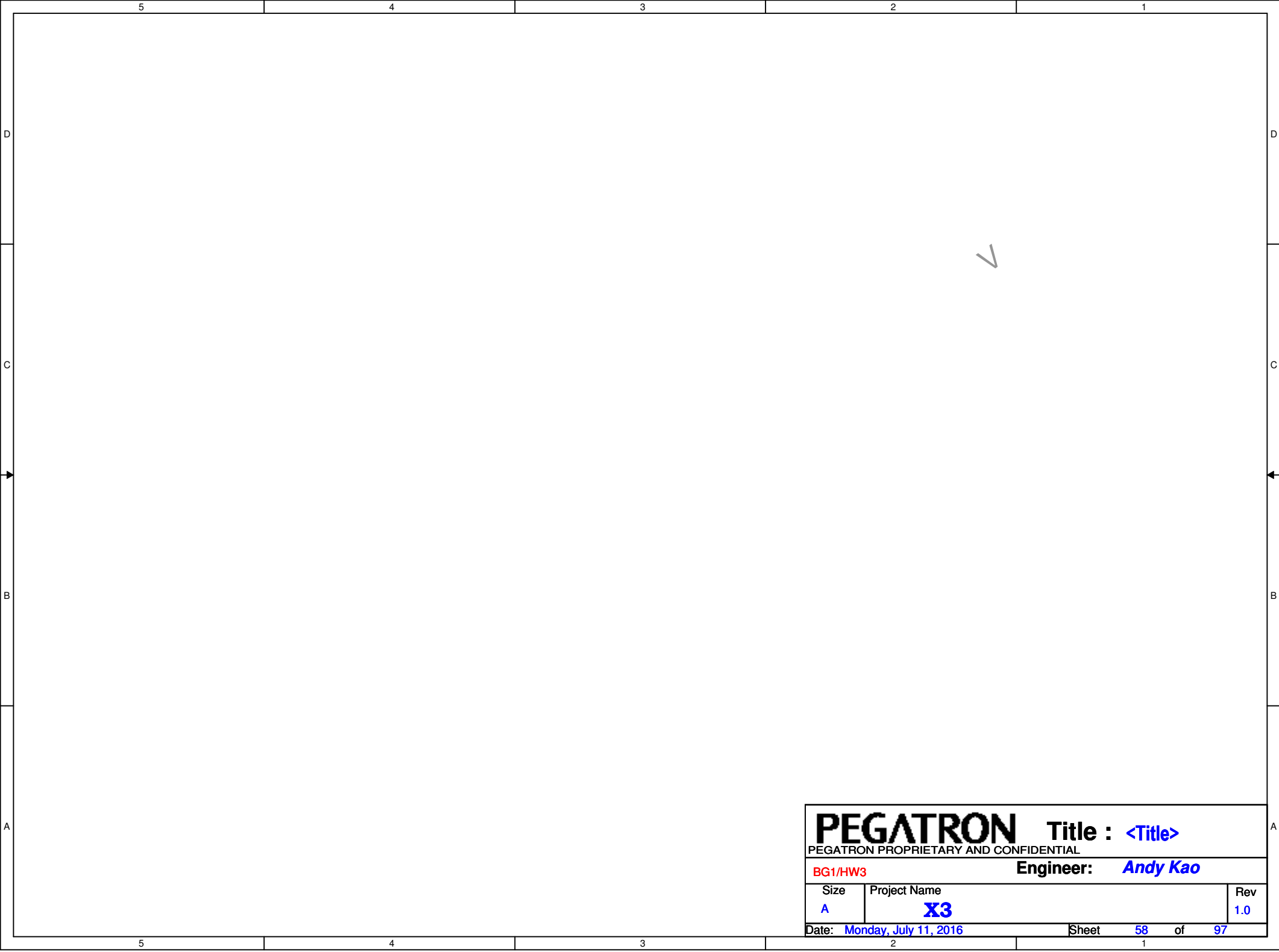


<Variant Name>

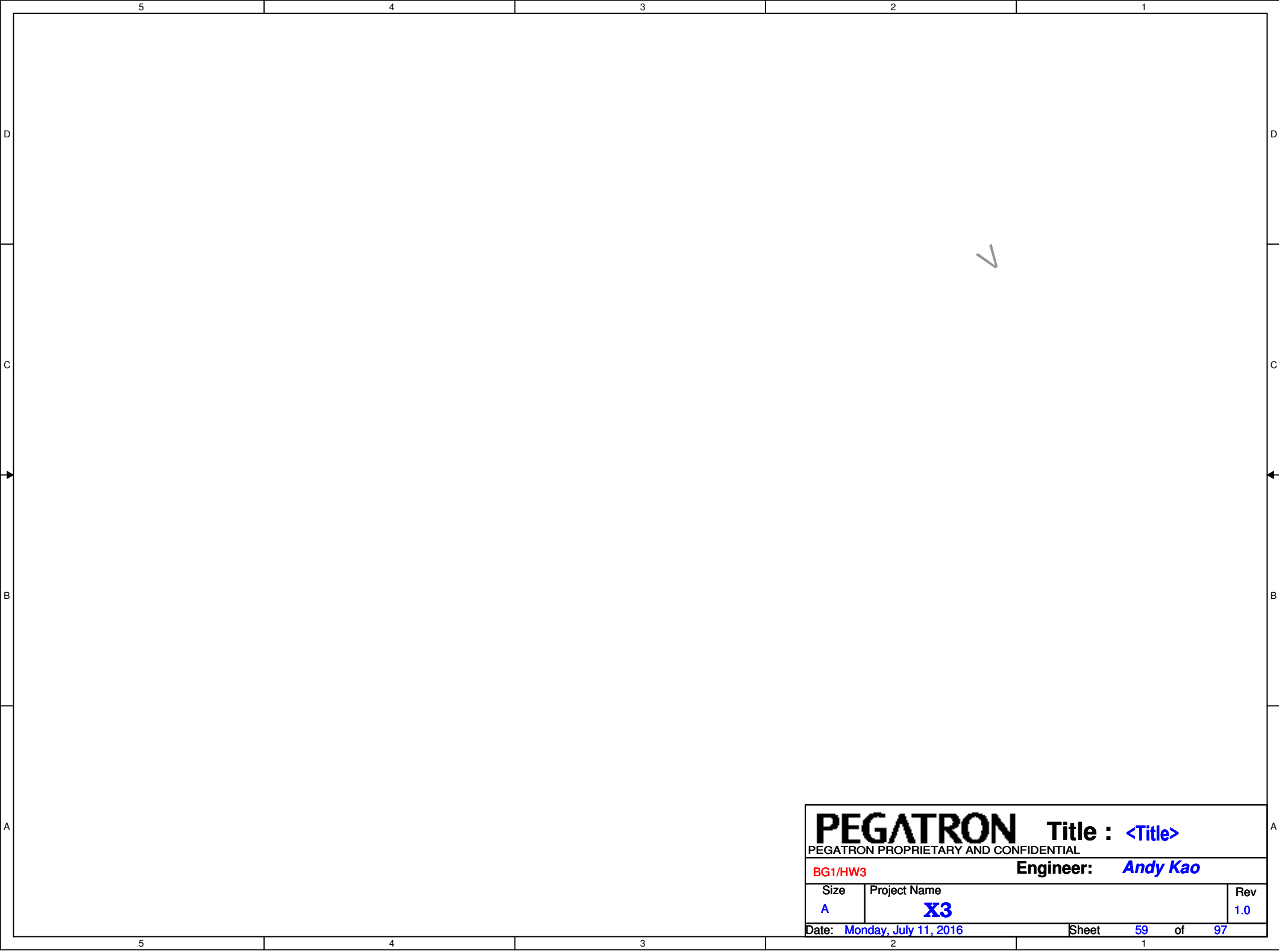
PEGATRON		Title : LED_Indicator	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 56 of 97	

Discharge Circuit



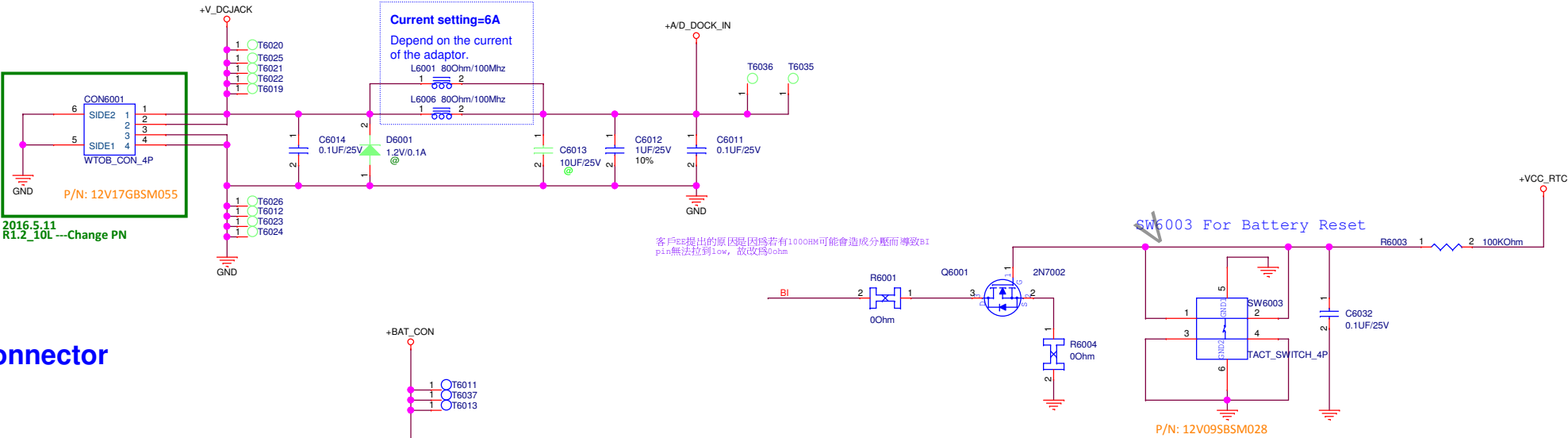


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 58 of 97	

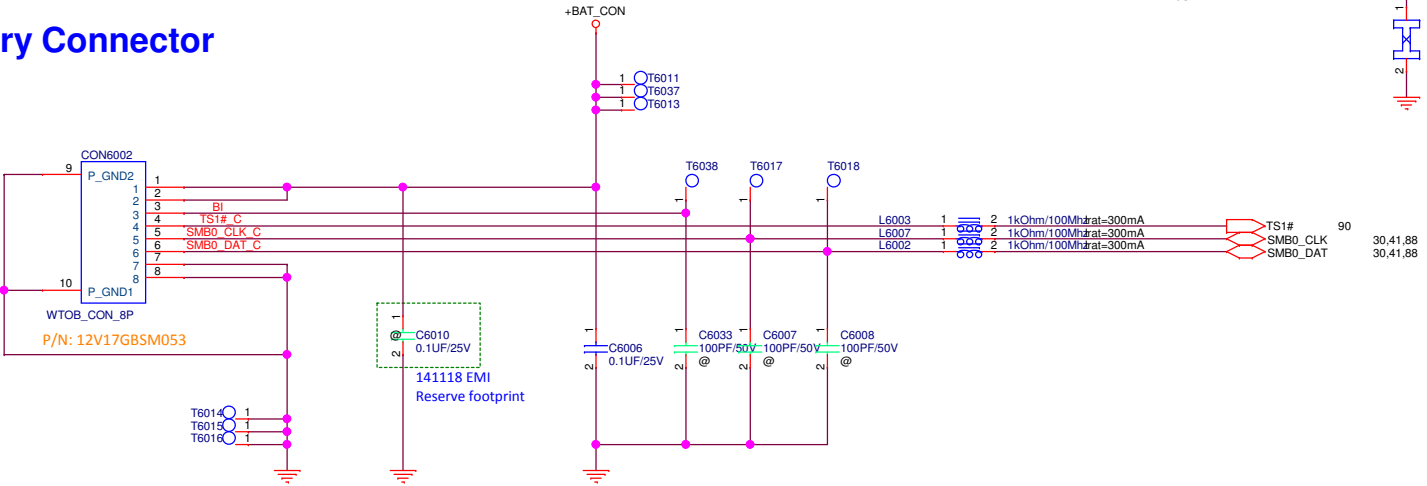


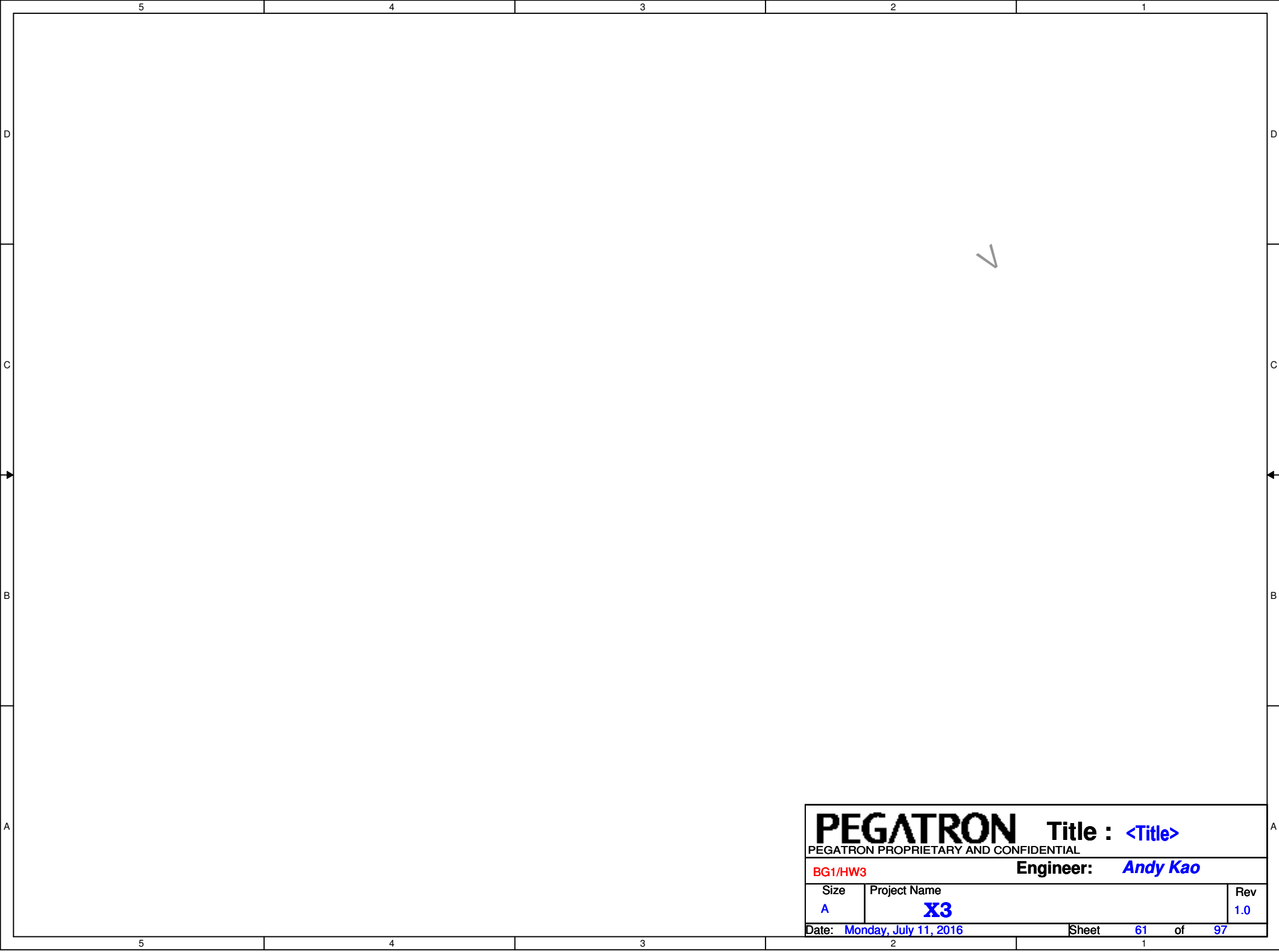
PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
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DC Jack WtoB CONN

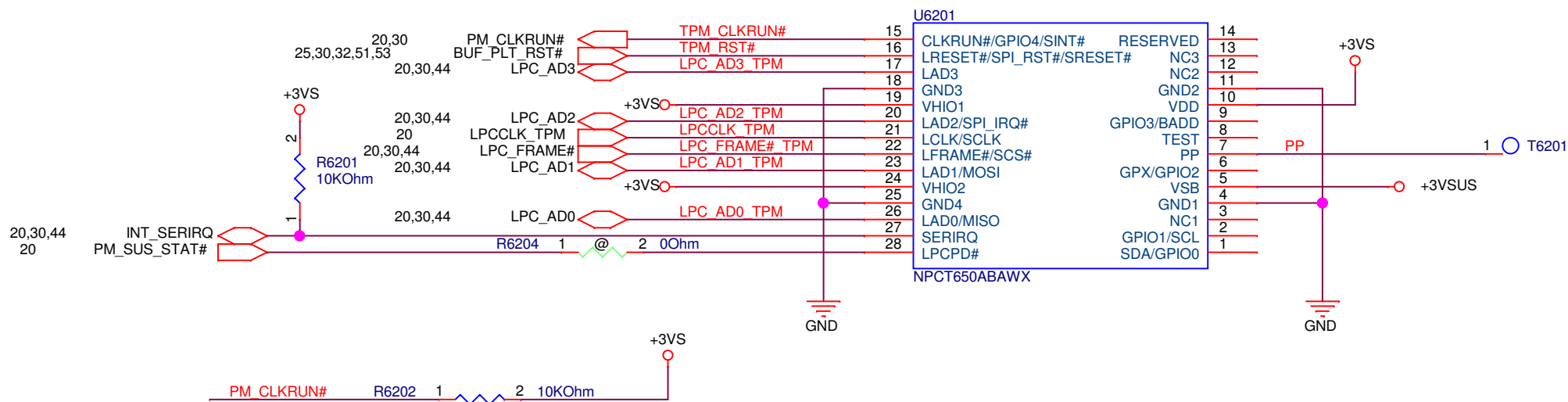
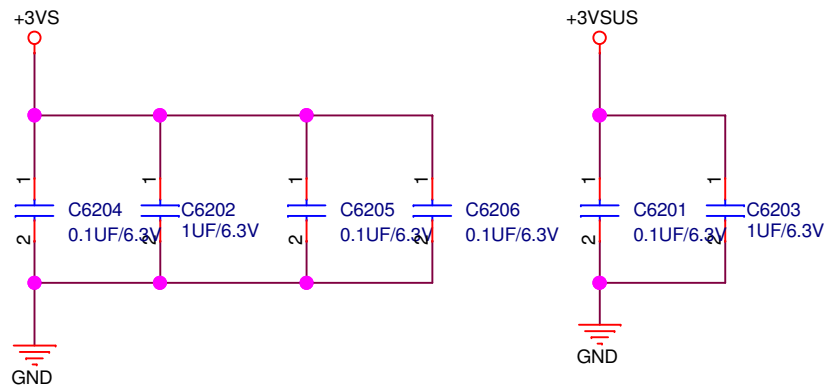


Battery Connector





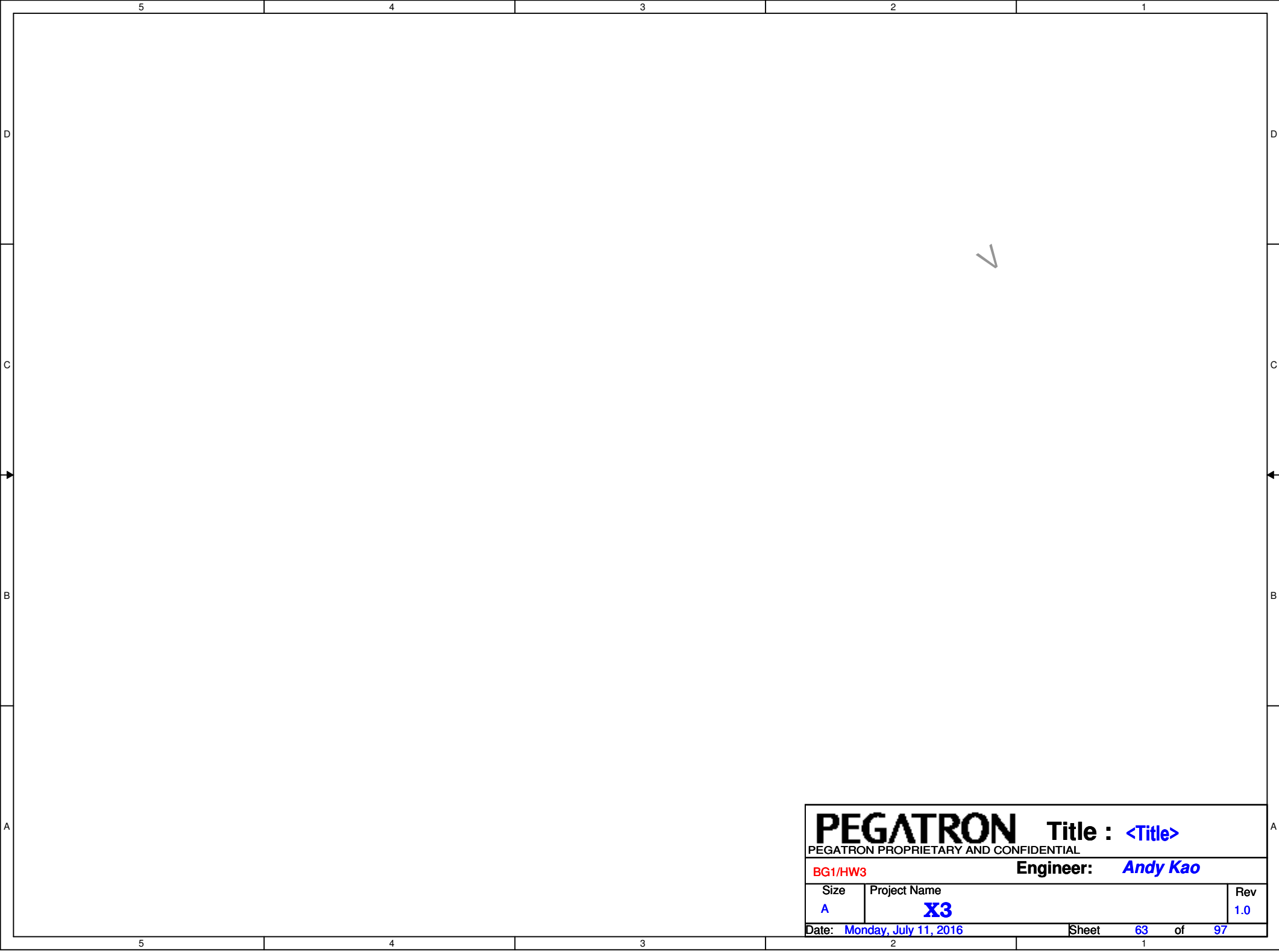
PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 61 of 97	



Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

PEGATRON		Title : TPM CONN	
BG1/HW3		Engineer: Andy Kao	
Size Custom	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet	62 of 97



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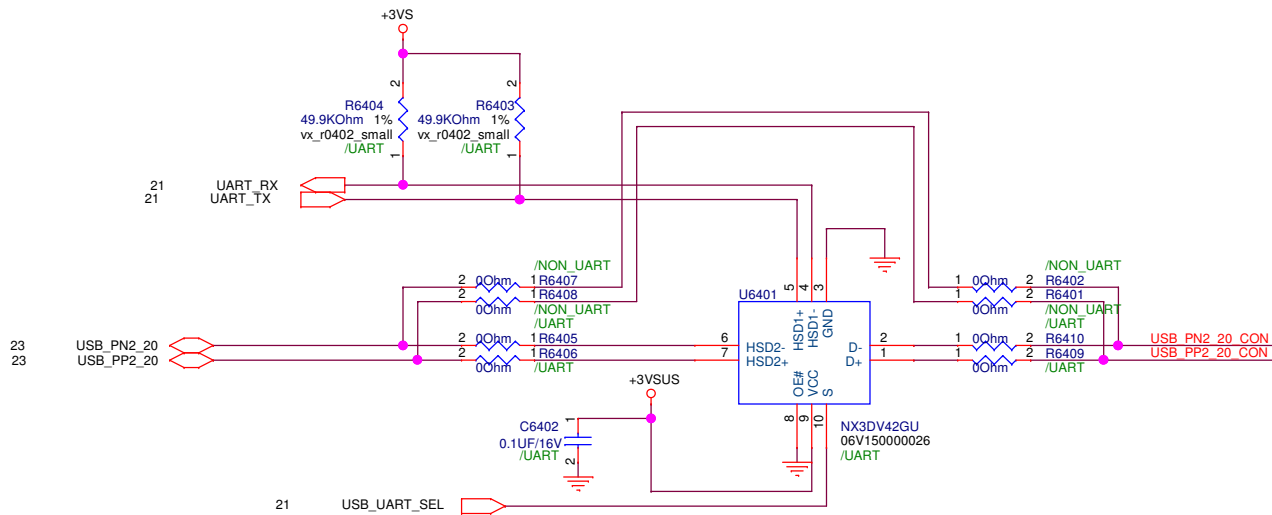
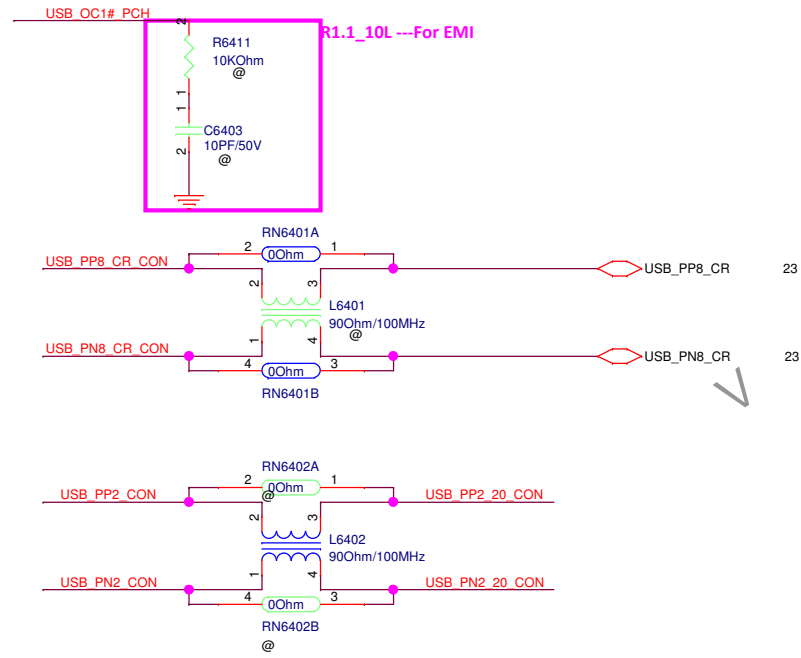
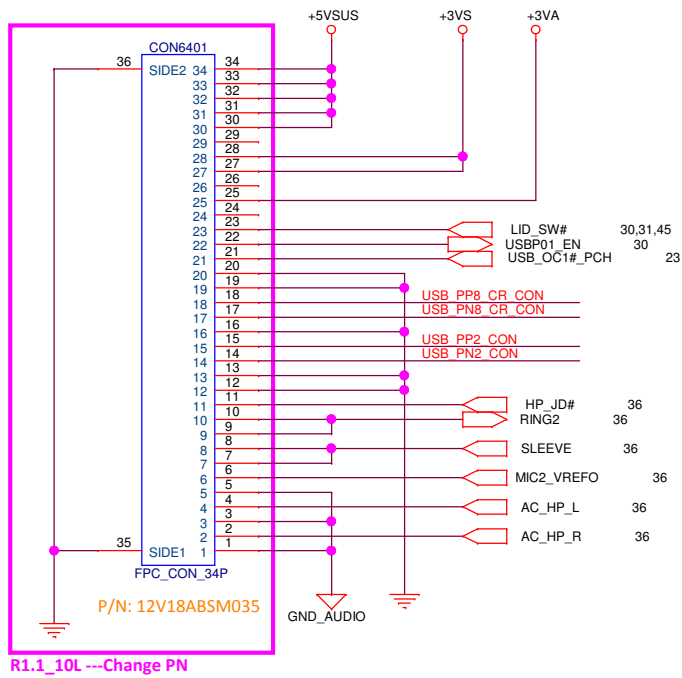
B

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PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 63 of 97

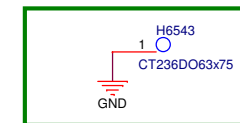
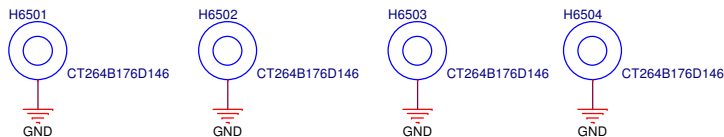


<Variant Name>		
PEGATRON Title : IO CON. PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3 Engineer: Andy Kao		
Size B	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016 Sheet 64 of 97		

CPU NUT

6*2.5mm*1

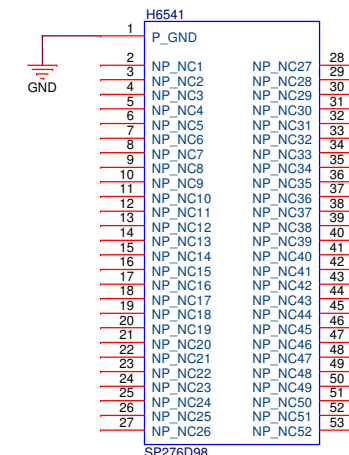
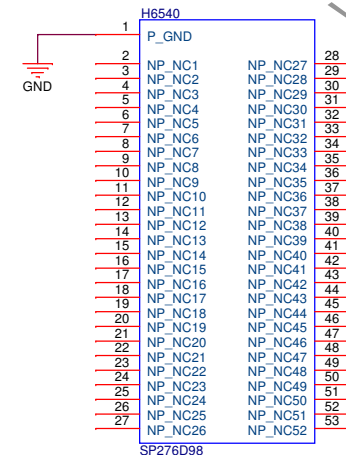
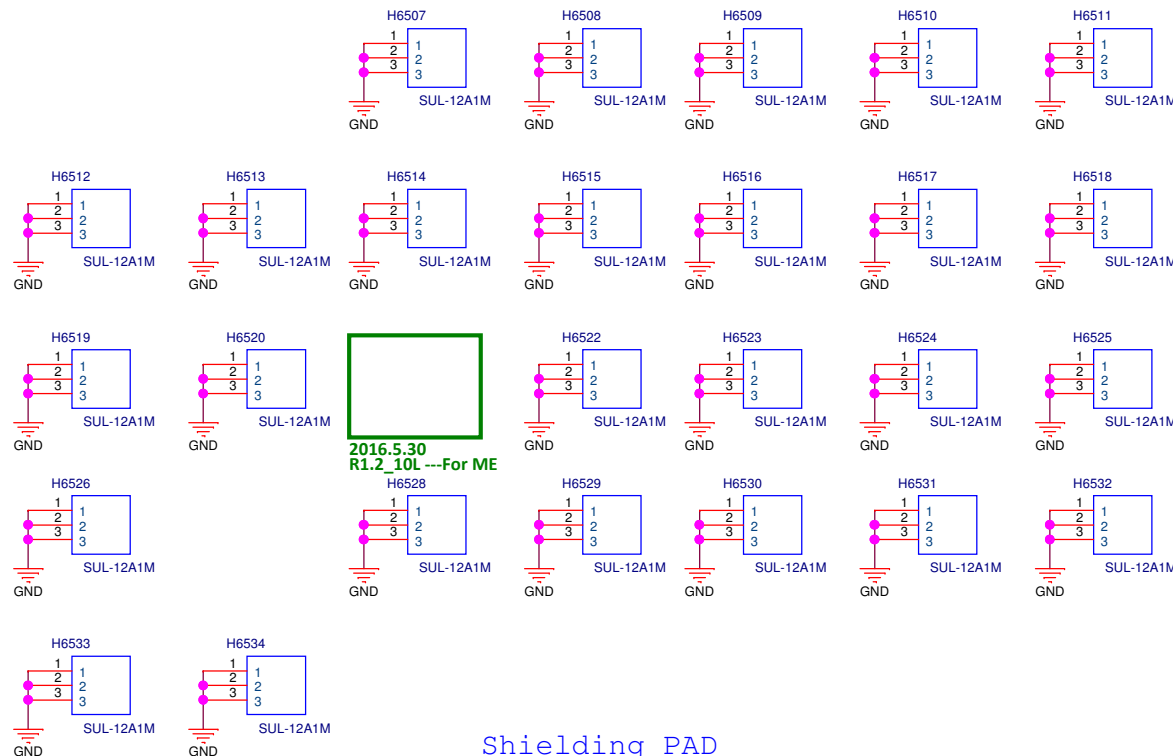
6*3.1mm*1



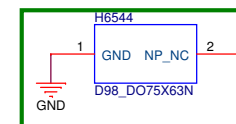
2016.6.6 R1.2_10L ---For ME

CLIP

Thermal screw*2

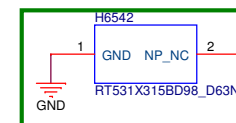


14*8mm*1



2016.6.6 R1.2_10L ---For ME

13.5*8mm*1

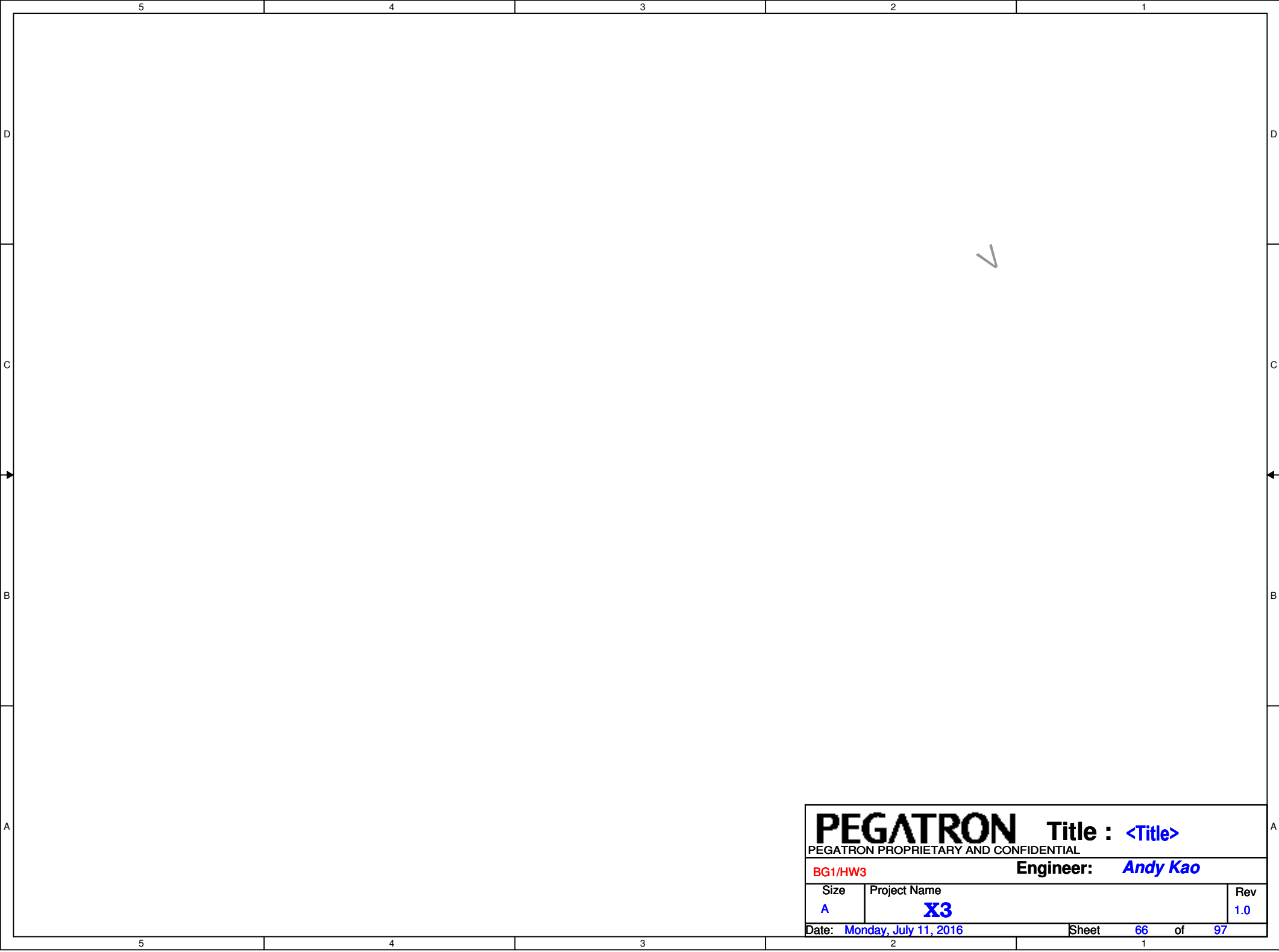


2016.6.6 R1.2_10L ---For ME

Shielding PAD



PEGATRON		Title : NUT,Screw Hole	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 65 of 97	



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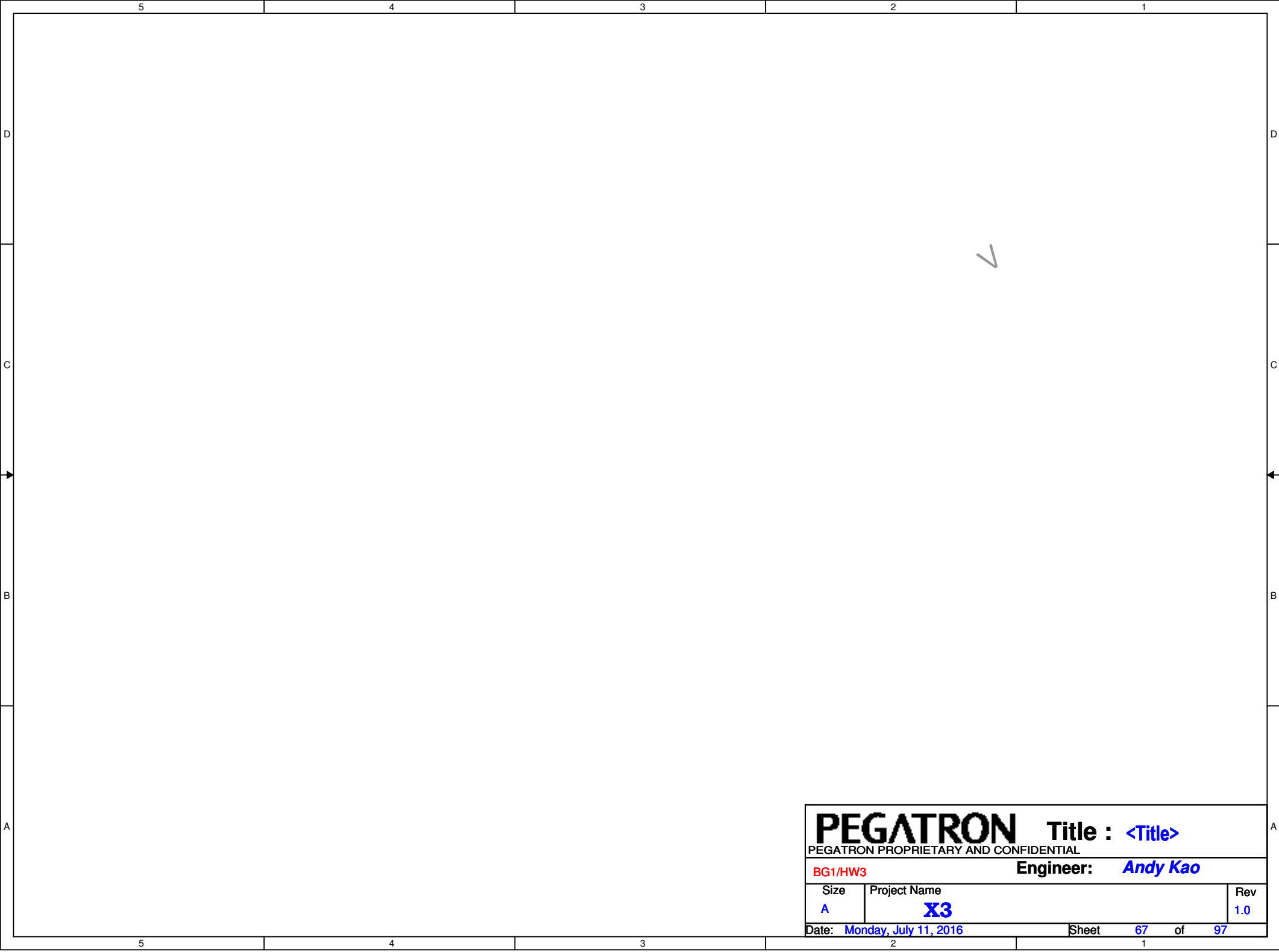
B

B

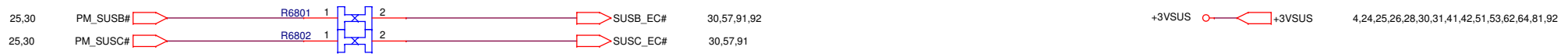
A

A

PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 66 of 97

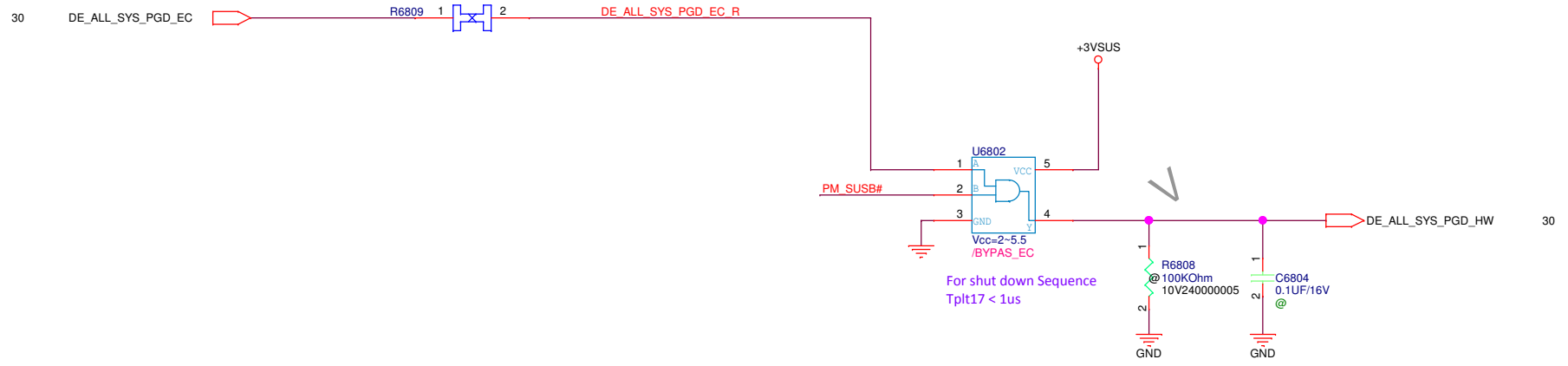


PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size A	Project Name X3	Rev 1.0
Date: Monday, July 11, 2016		Sheet 67 of 97

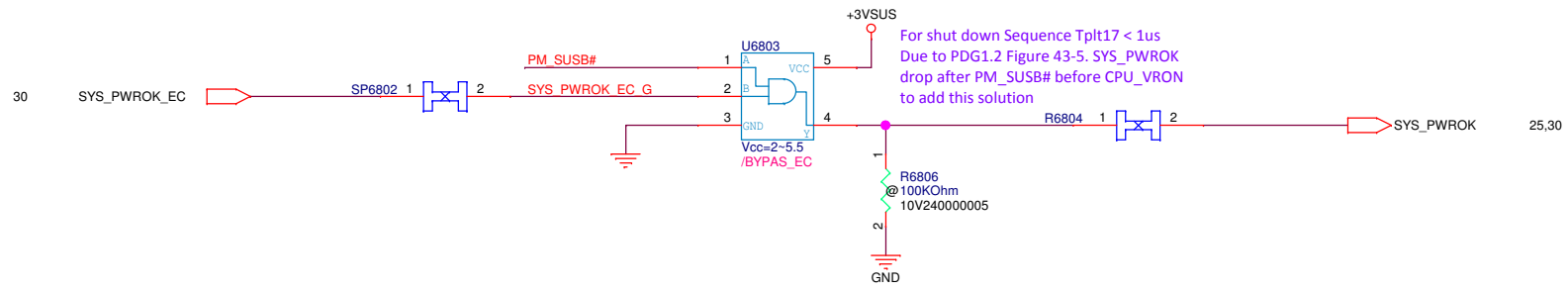


For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

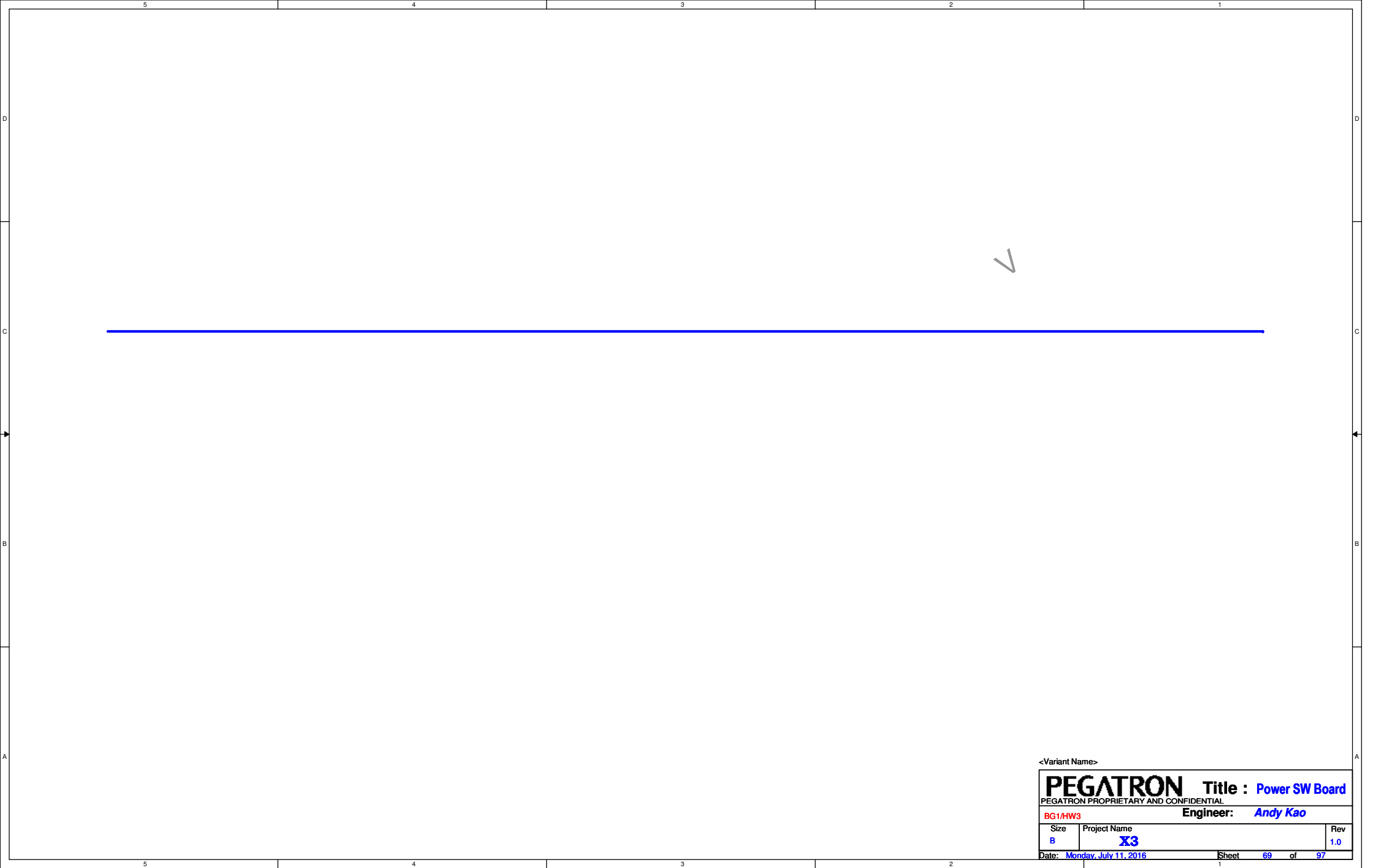
Delay By EC(2ms+ EC processing time (3ms~33ms))



For shut down Sequence
Tplt17 < 1us

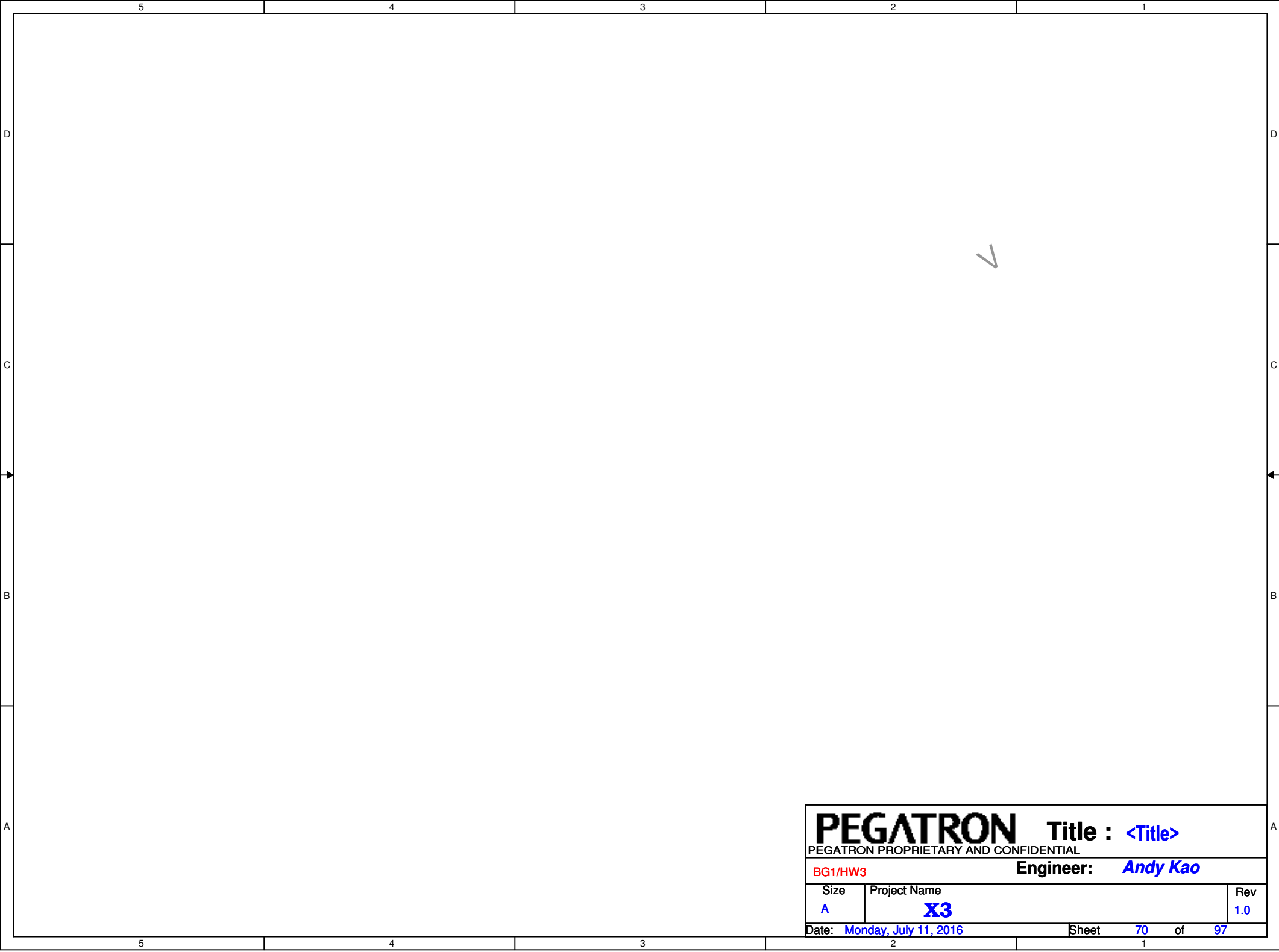


For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK
drop after PM_SUSB# before CPU_VRON
to add this solution



<Variant Name>

PEGATRON		Title : Power SW Board	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size	Project Name		Rev
B	X3		1.0
Date: Monday, July 11, 2016		Sheet	69 of 97



PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

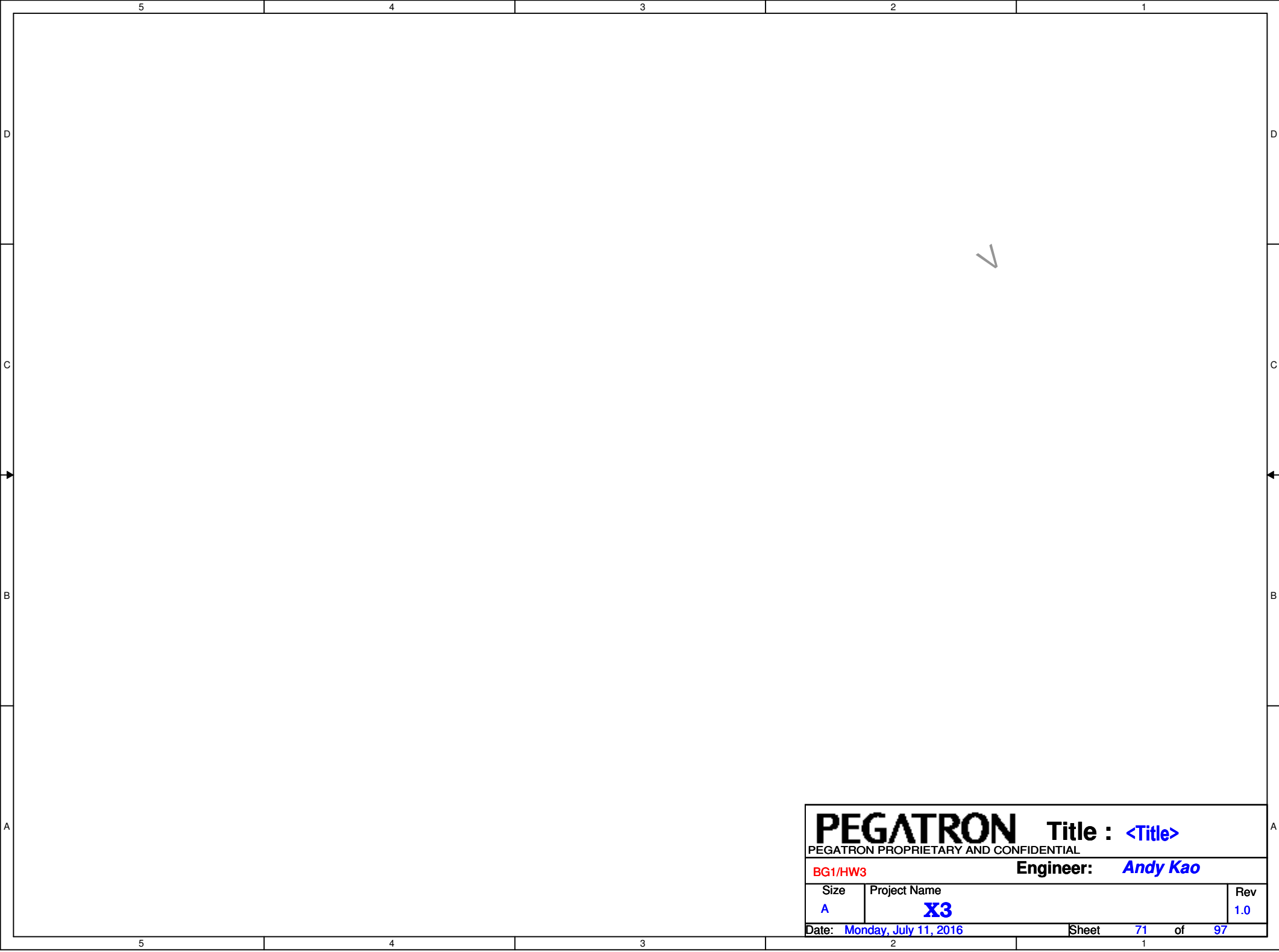
BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016

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D

D

C

C

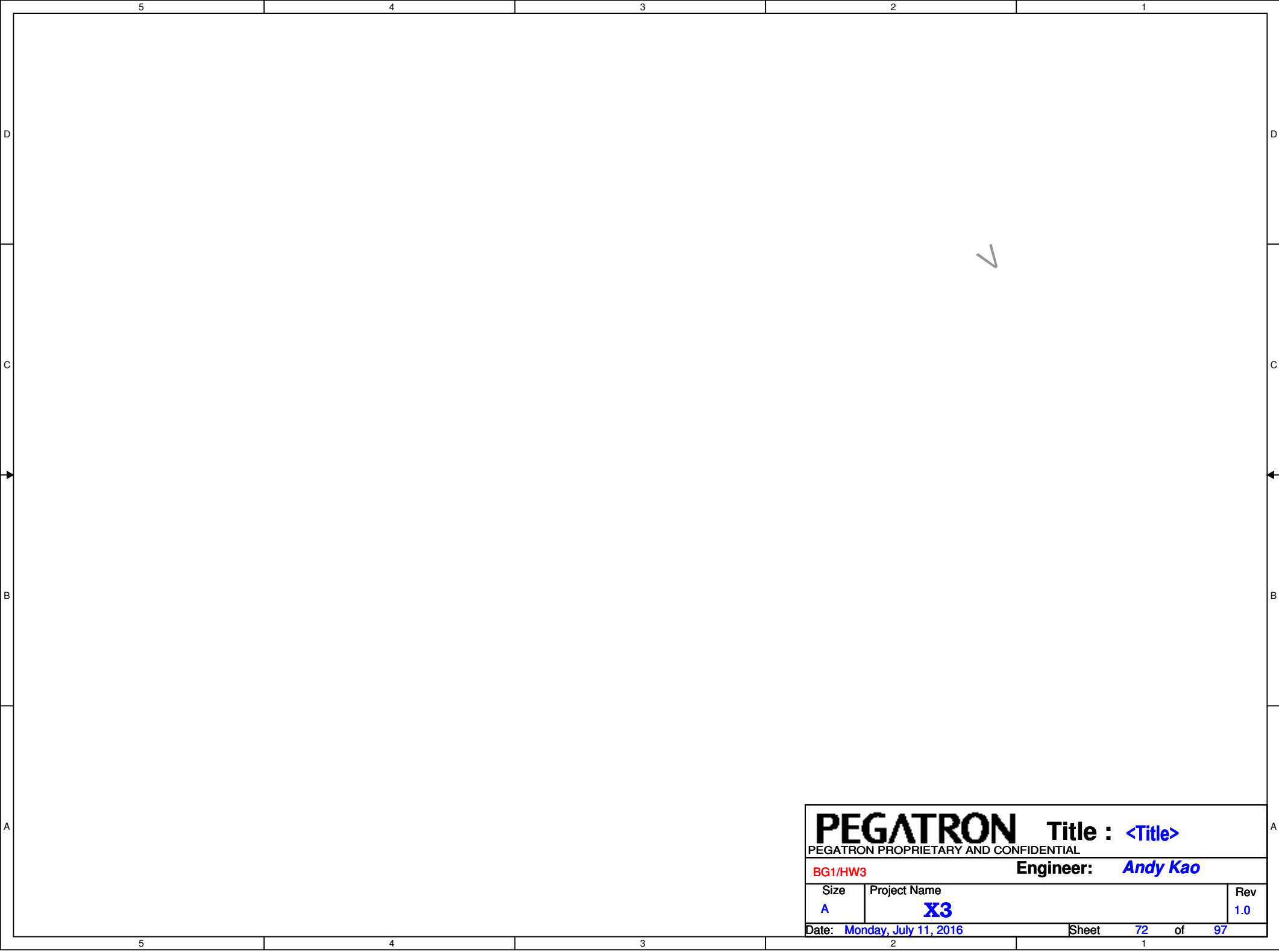
B

B

A

A

<div><div>PEGATRON</div><div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div></div>			Title : <Title>		
BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
Date: Monday, July 11, 2016			Sheet	71	of 97



D

D

C

C

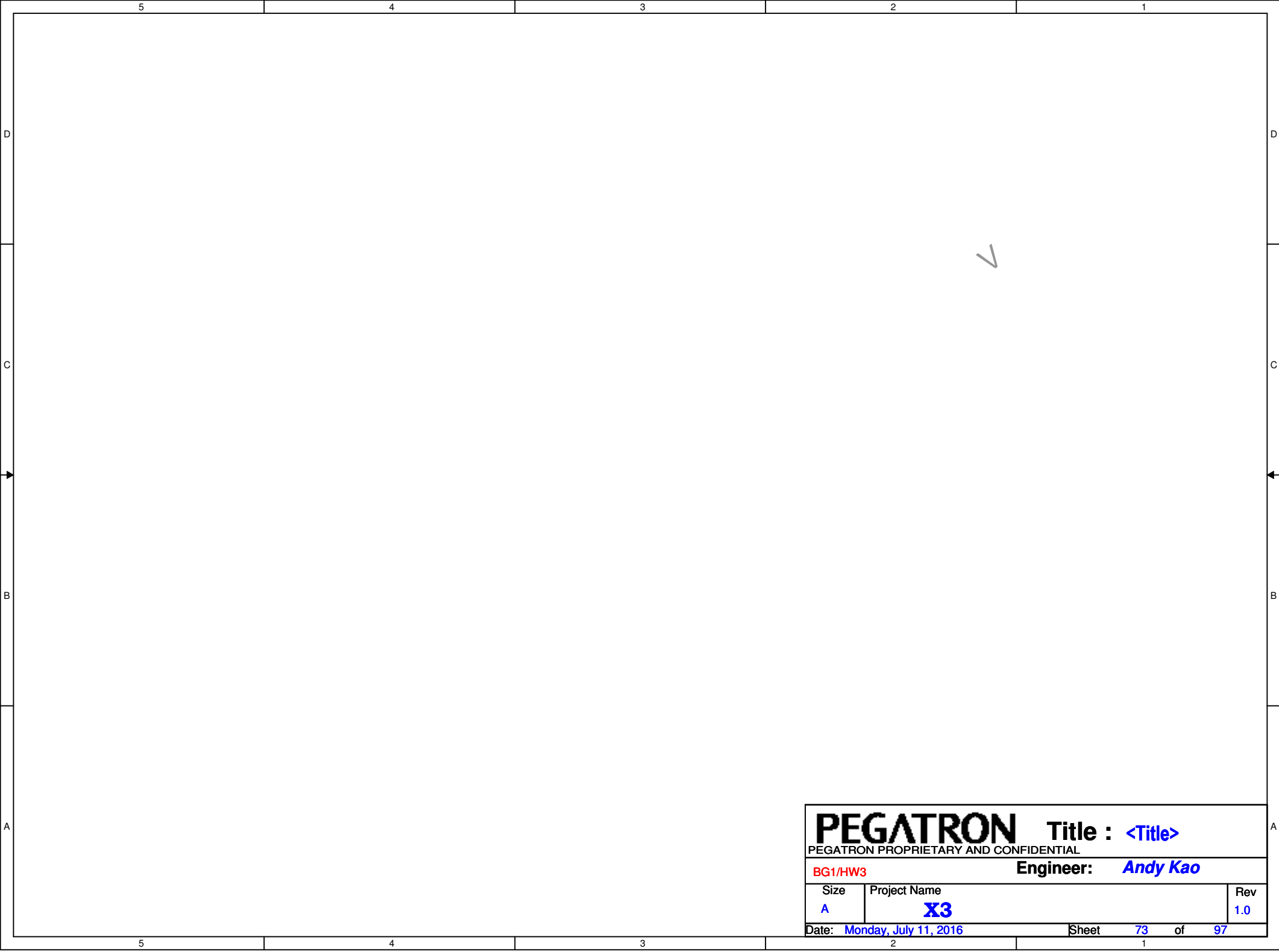
B

B

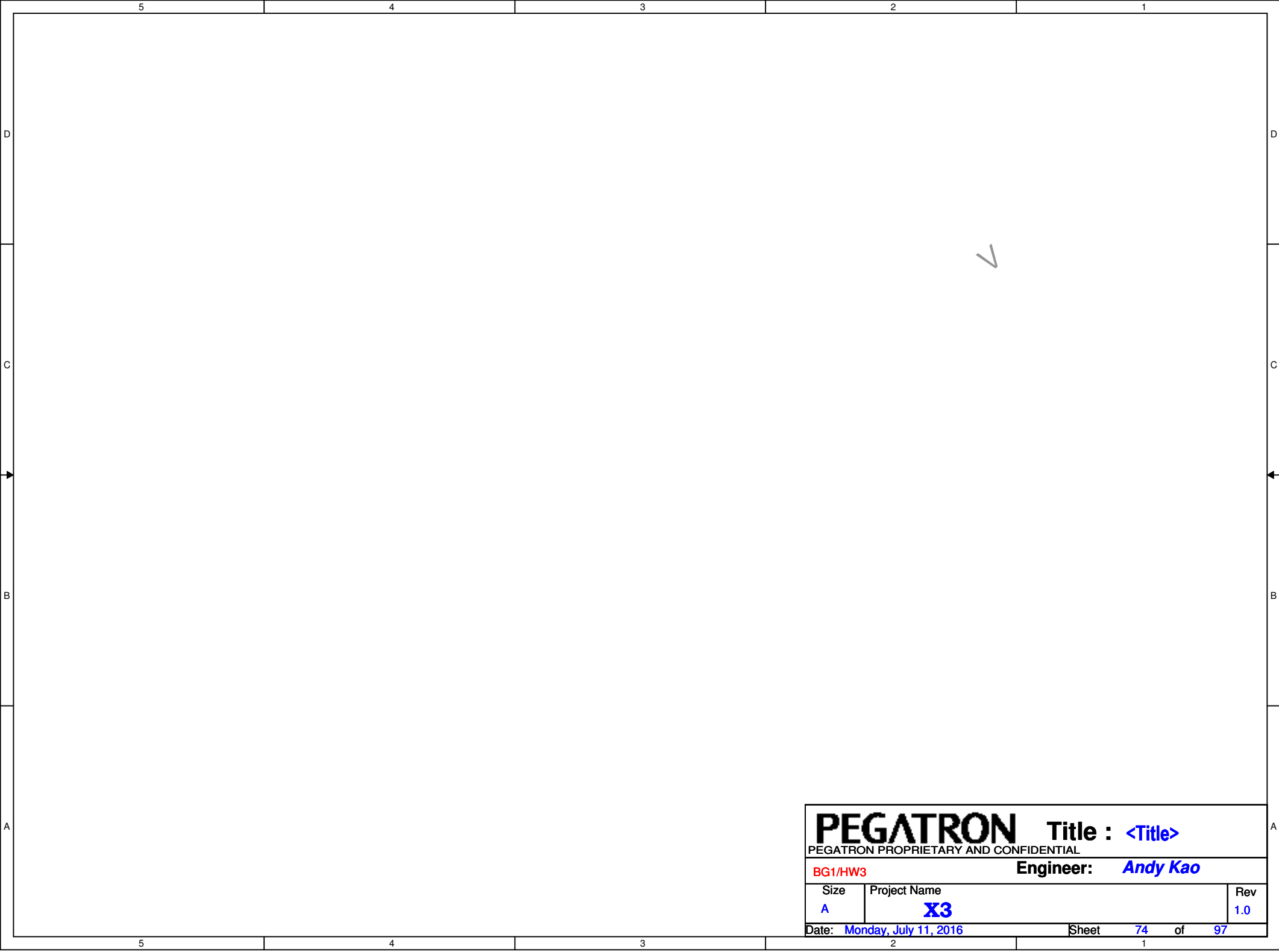
A

A

<div><div>PEGATRON</div><div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div></div>			Title : <Title>		
BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
Date: Monday, July 11, 2016			Sheet	72	of 97



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>73</i> of <i>97</i>



PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

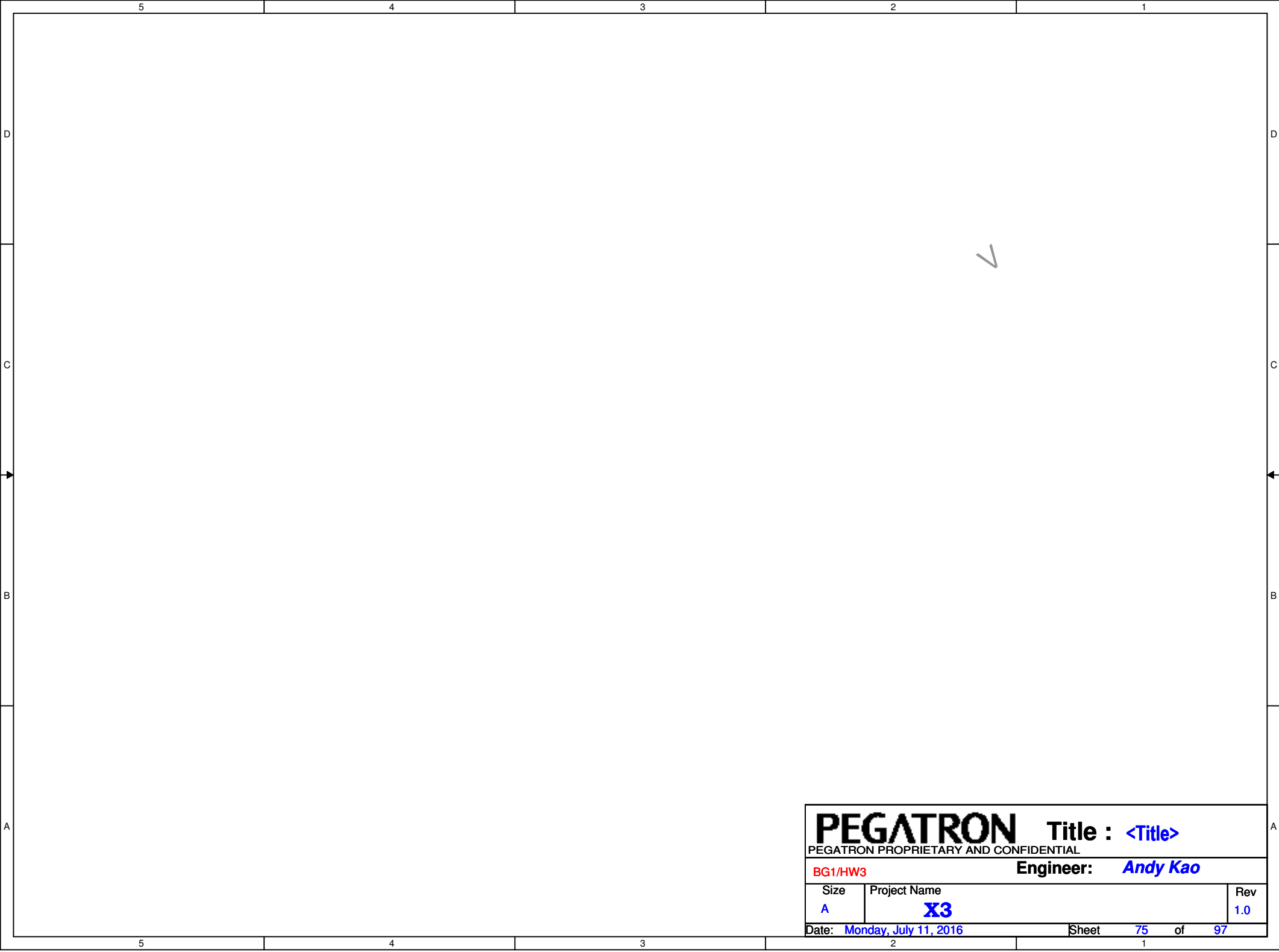
BG1/HW3

Engineer: Andy Kao

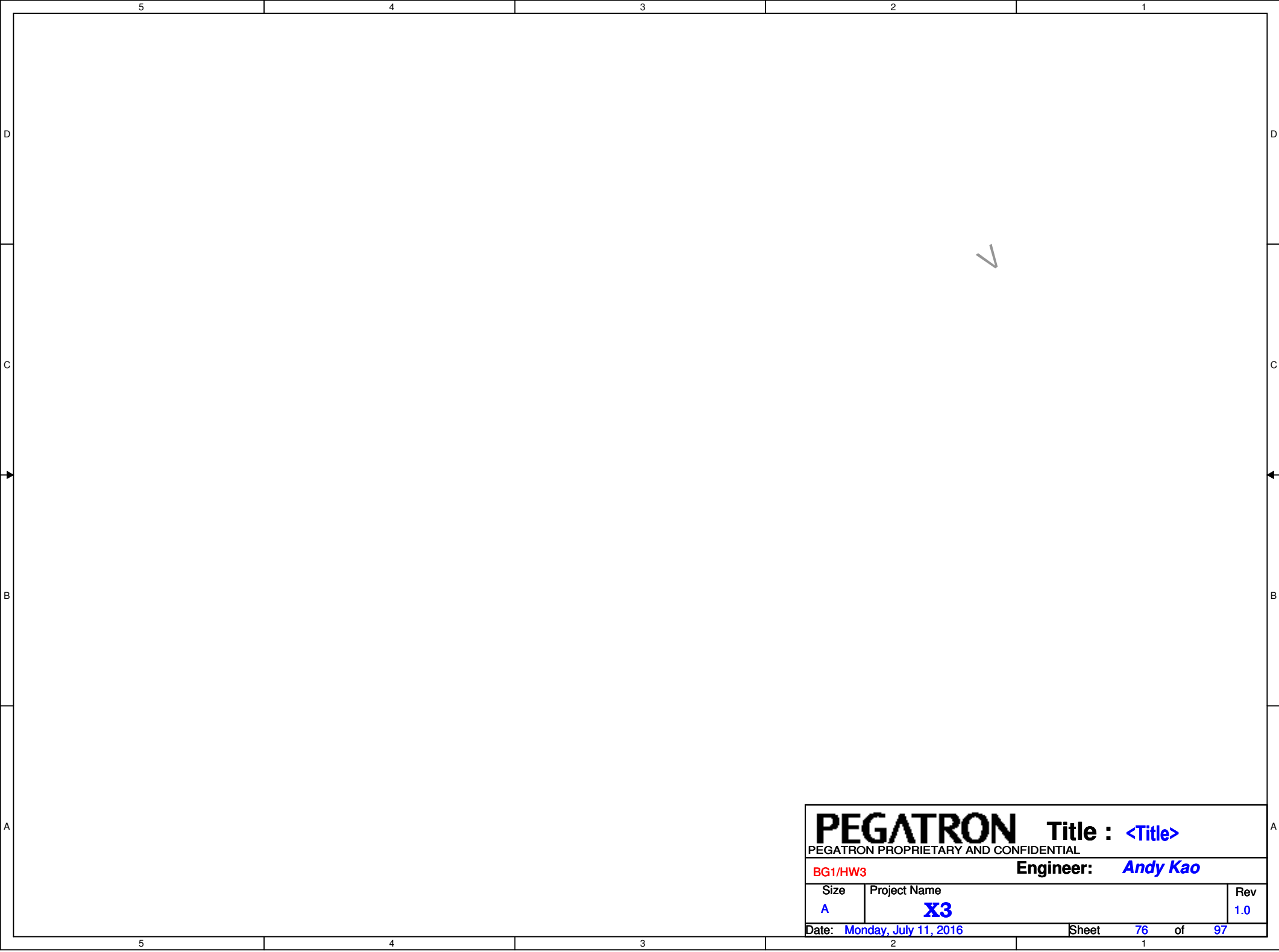
Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016

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PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>75</i> of <i>97</i>



D

D

C

C

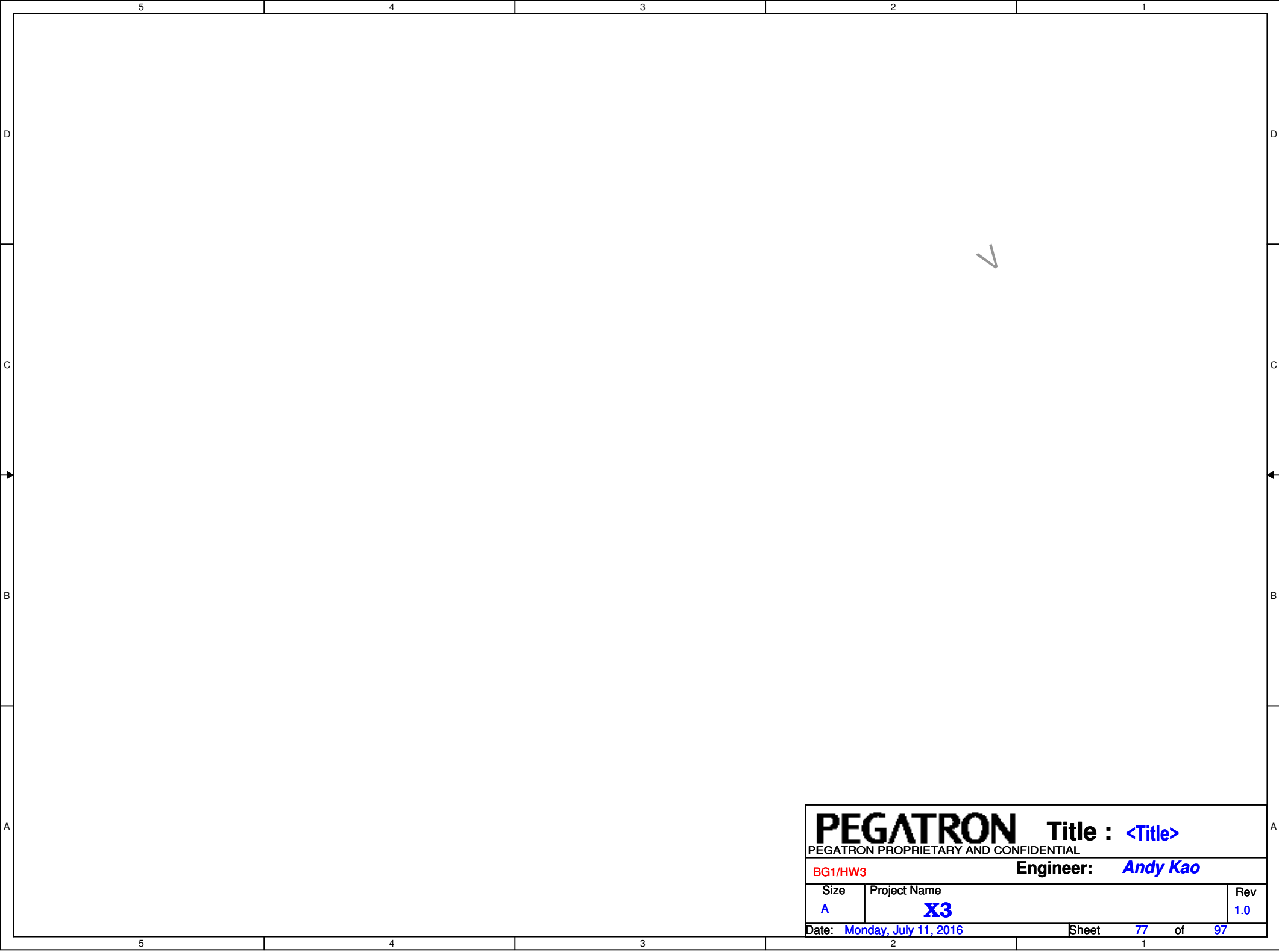
B

B

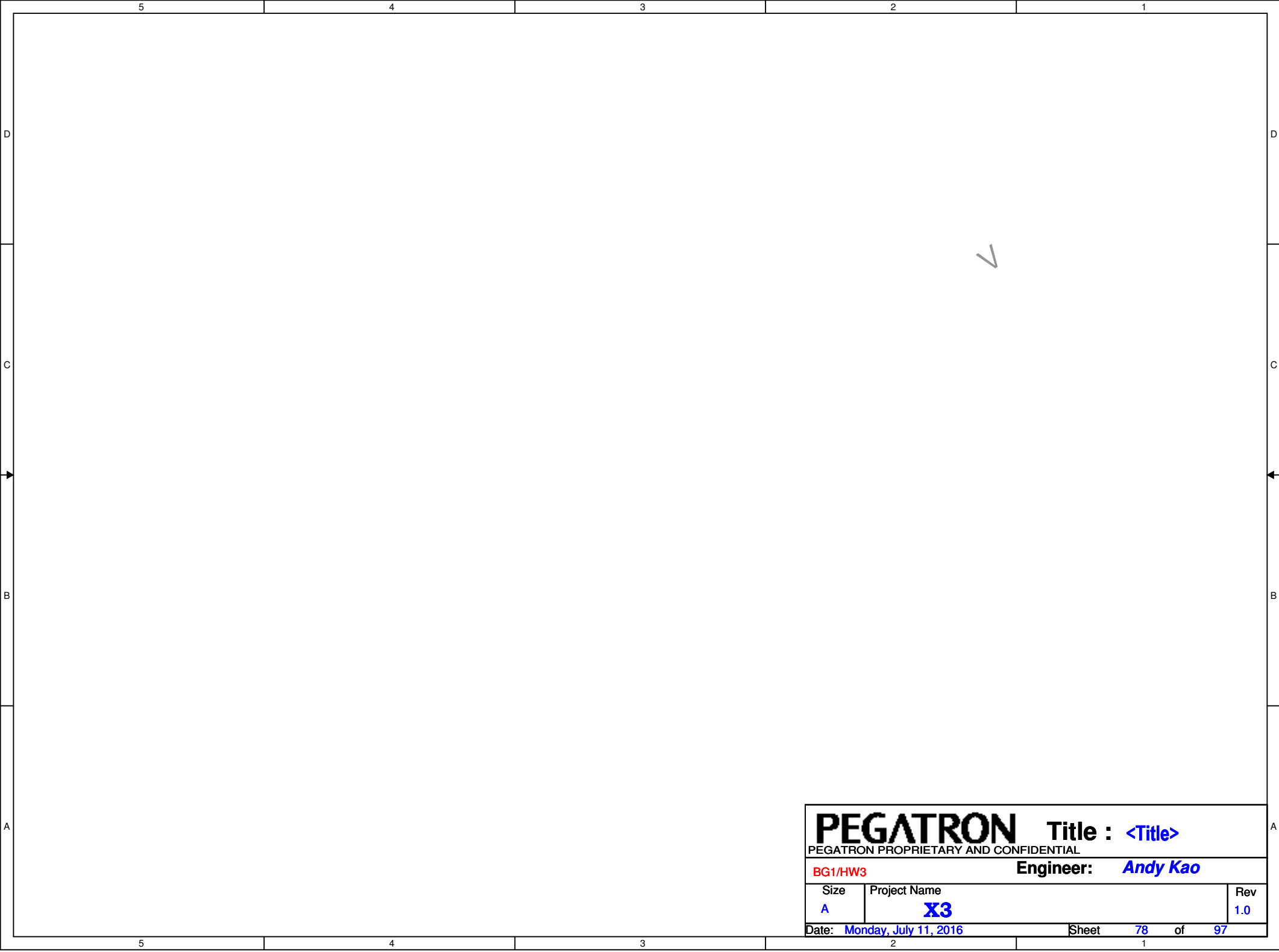
A

A

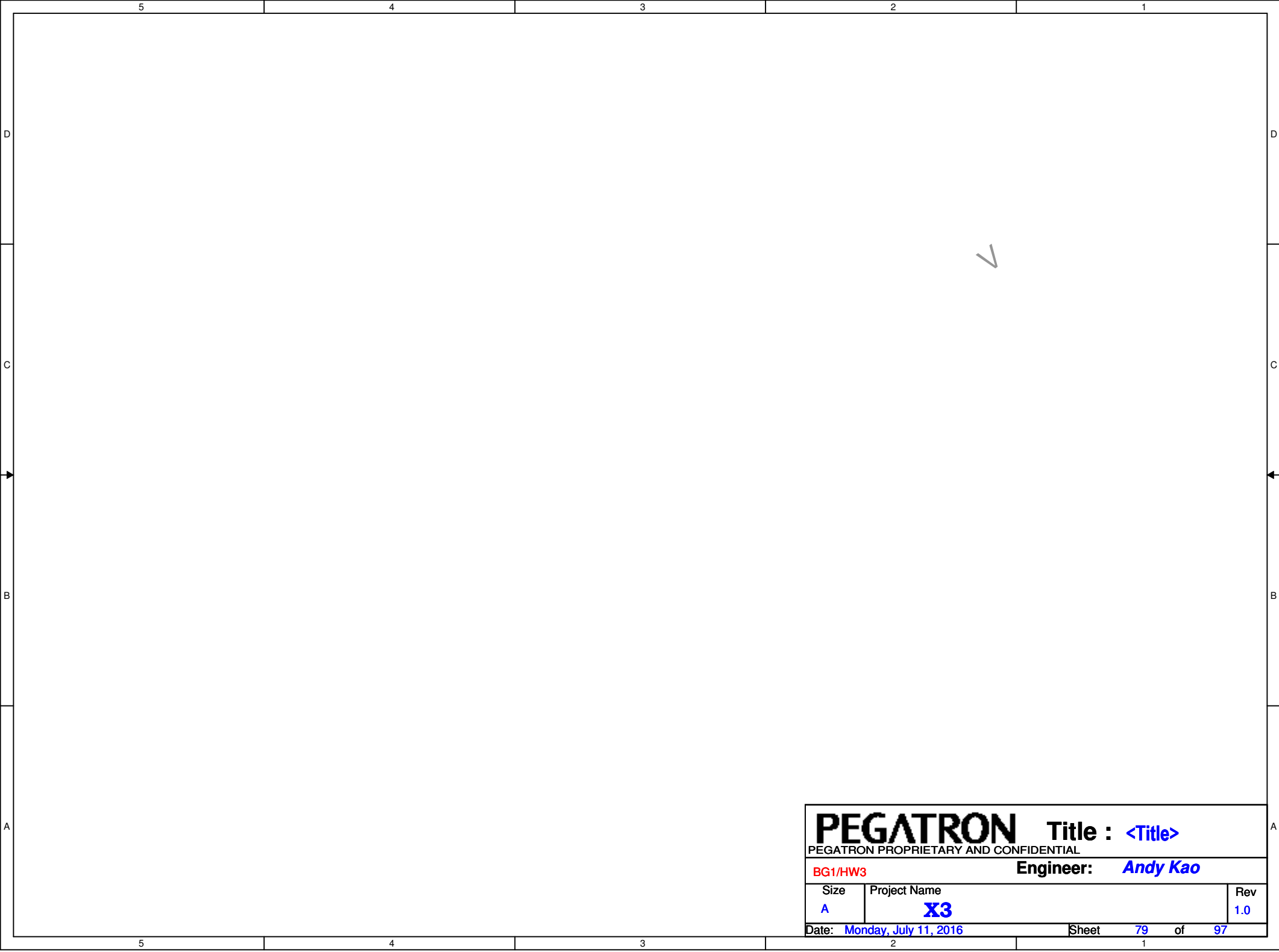
<div><div>PEGATRON</div><div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div></div>			Title : <Title>		
BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
Date: Monday, July 11, 2016			Sheet	76	of 97



PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>77</i> of <i>97</i>

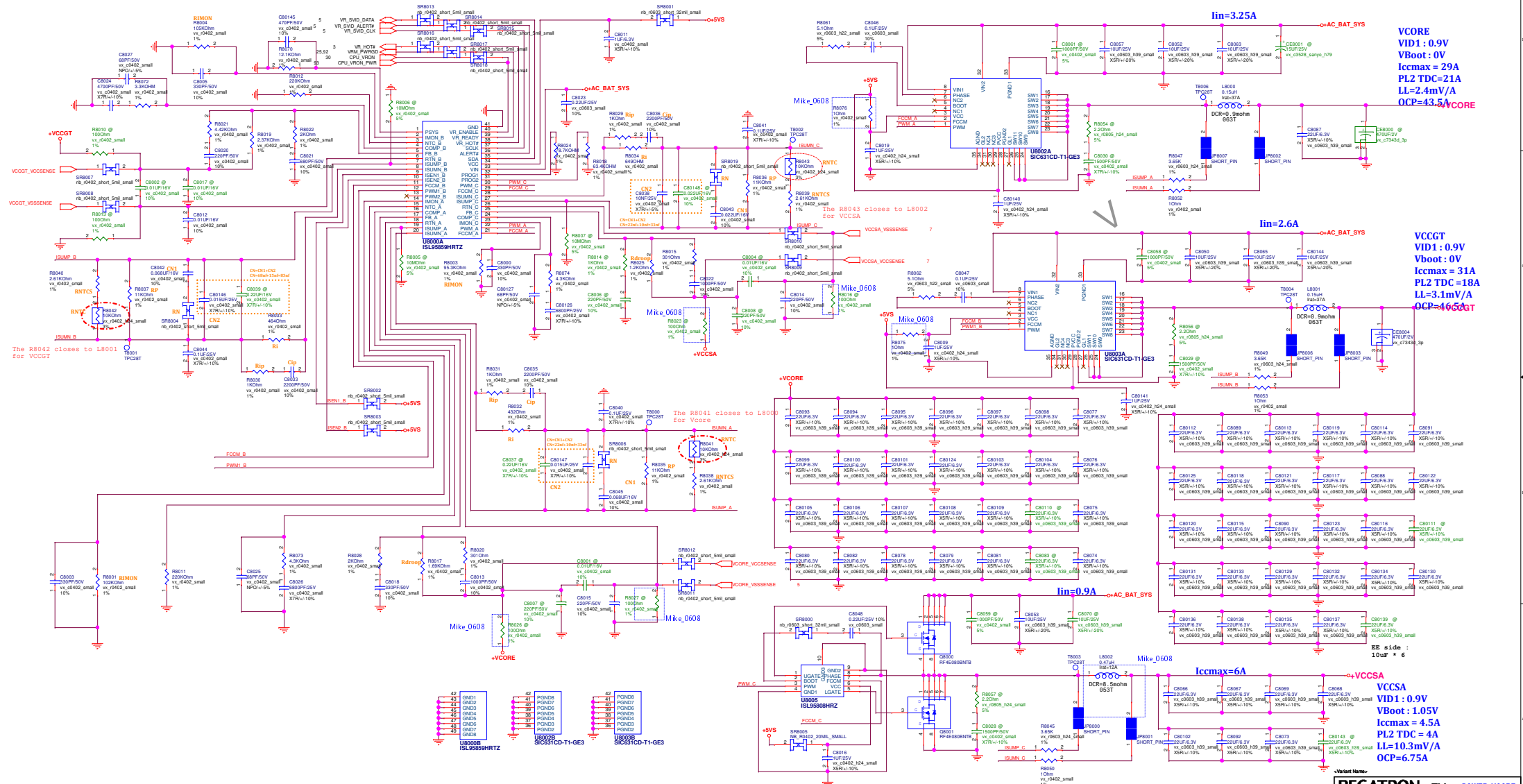


PEGATRON		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 78 of 97	

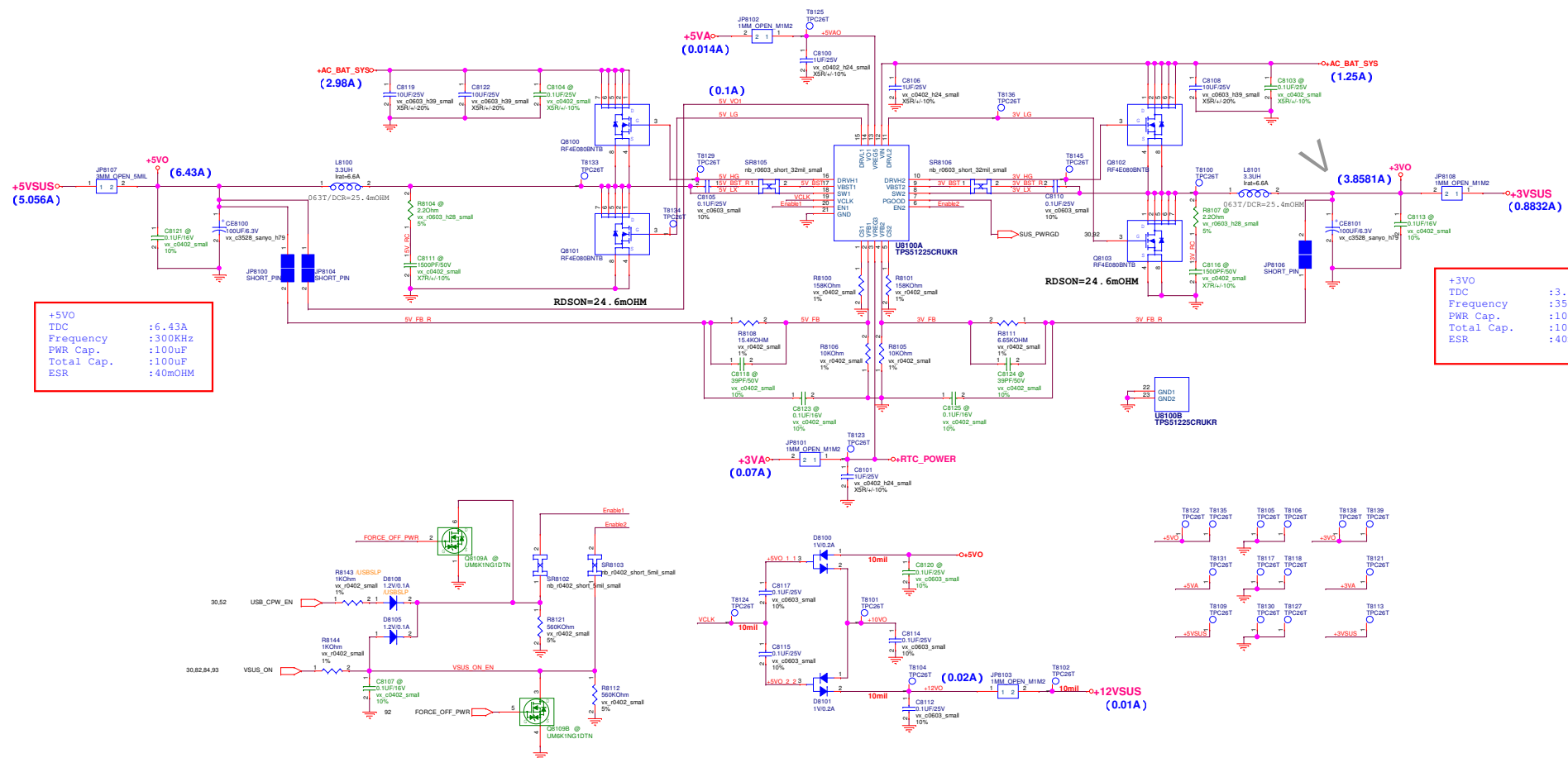


PEGATRON Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name X3	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>79</i> of <i>97</i>

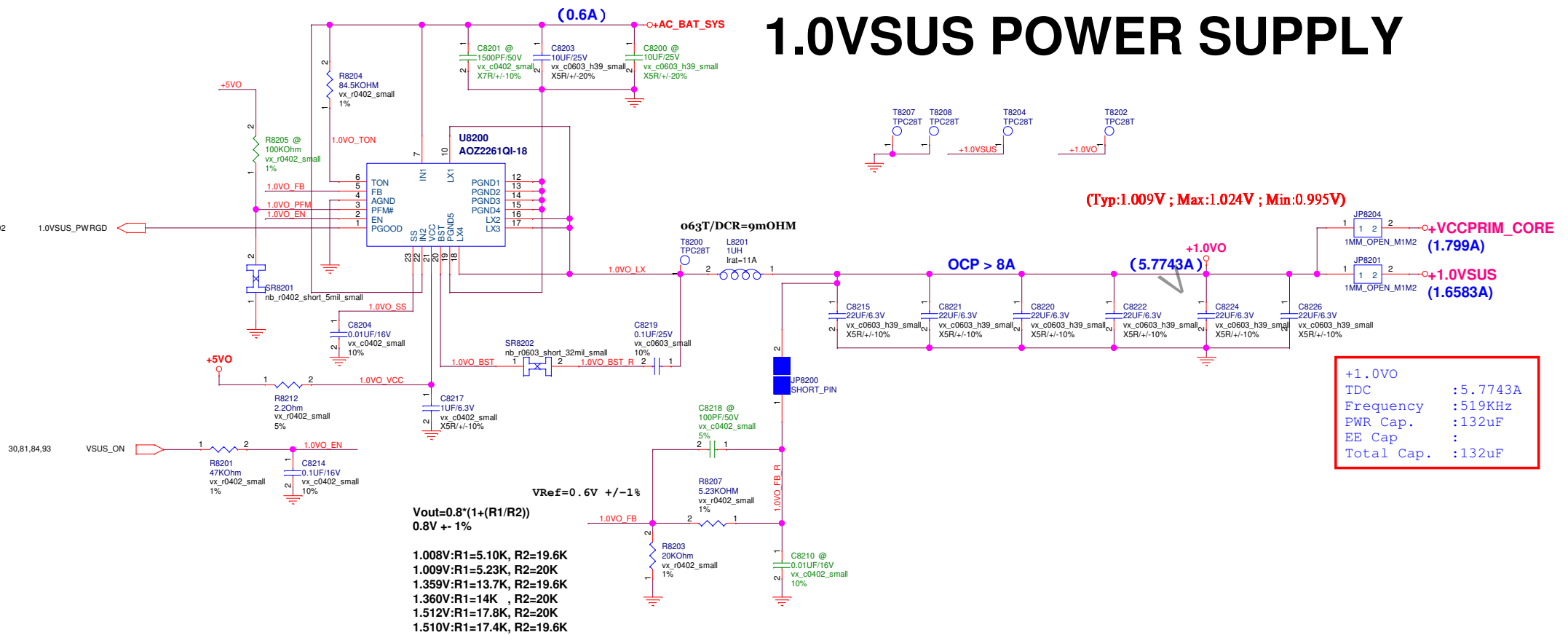
VCORE & VCCGT & VCCSA POWER SUPPLY



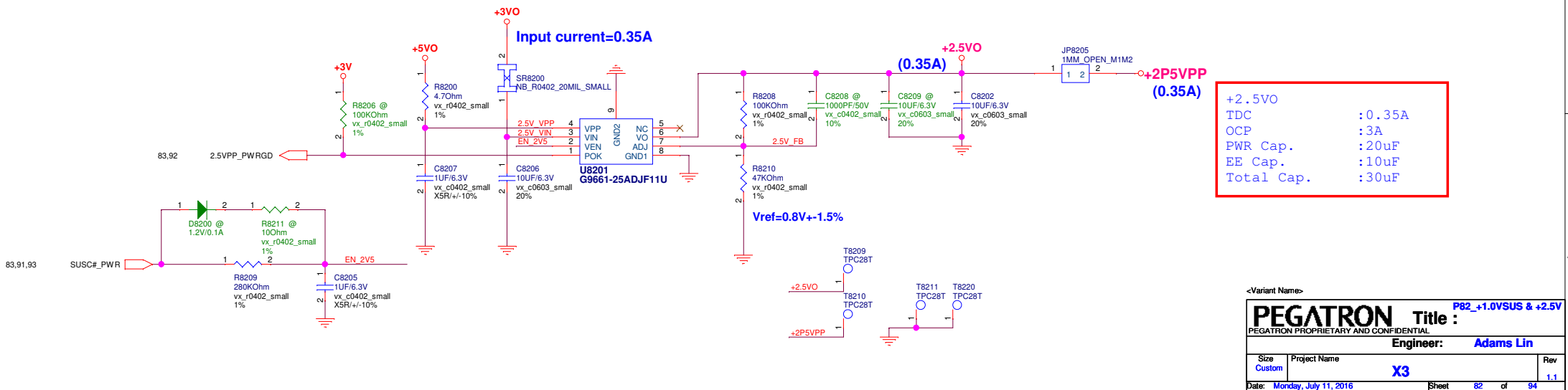
5VO & 3VO POWER SUPPLY



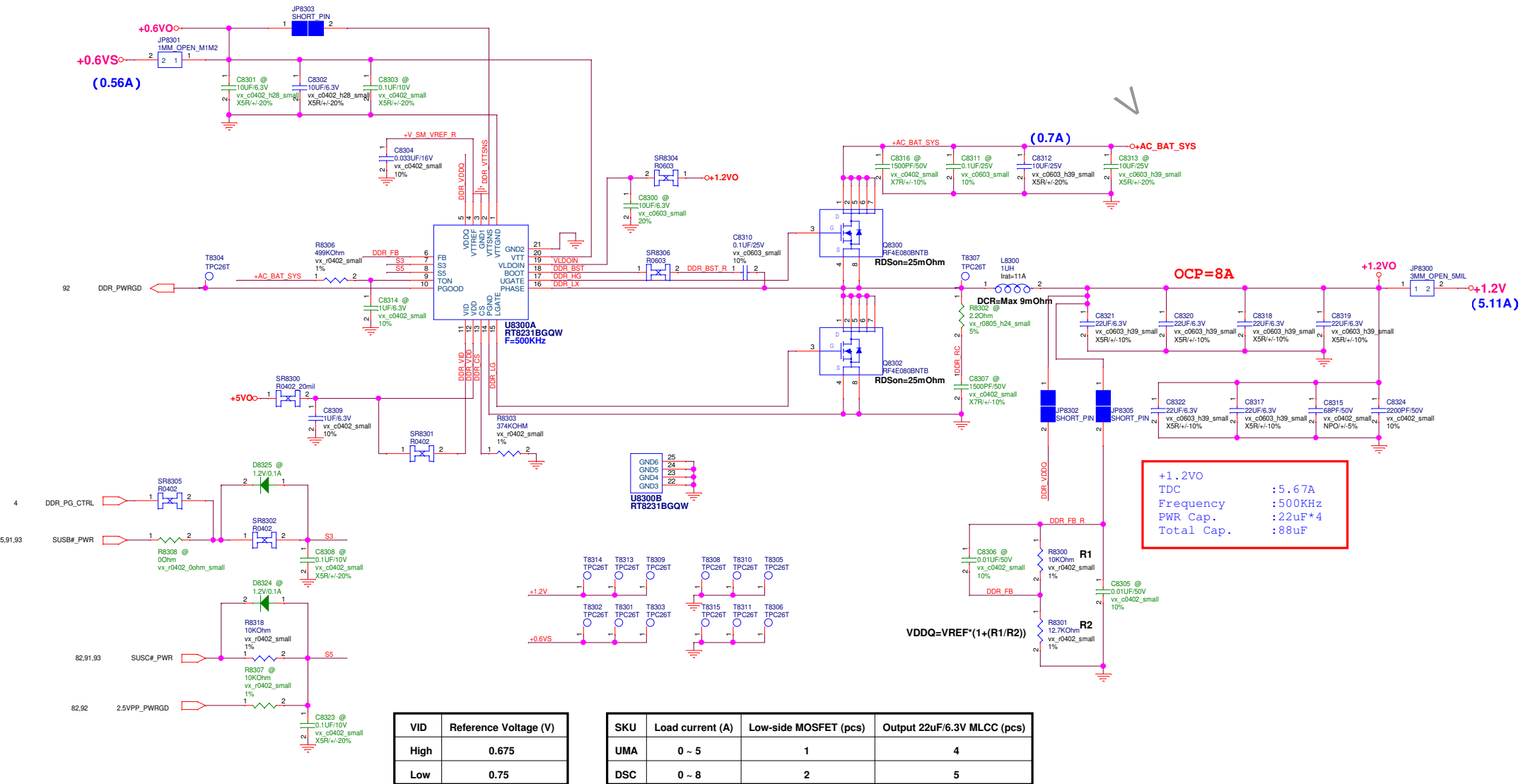
1.0VSUS POWER SUPPLY



2.5V POWER SUPPLY



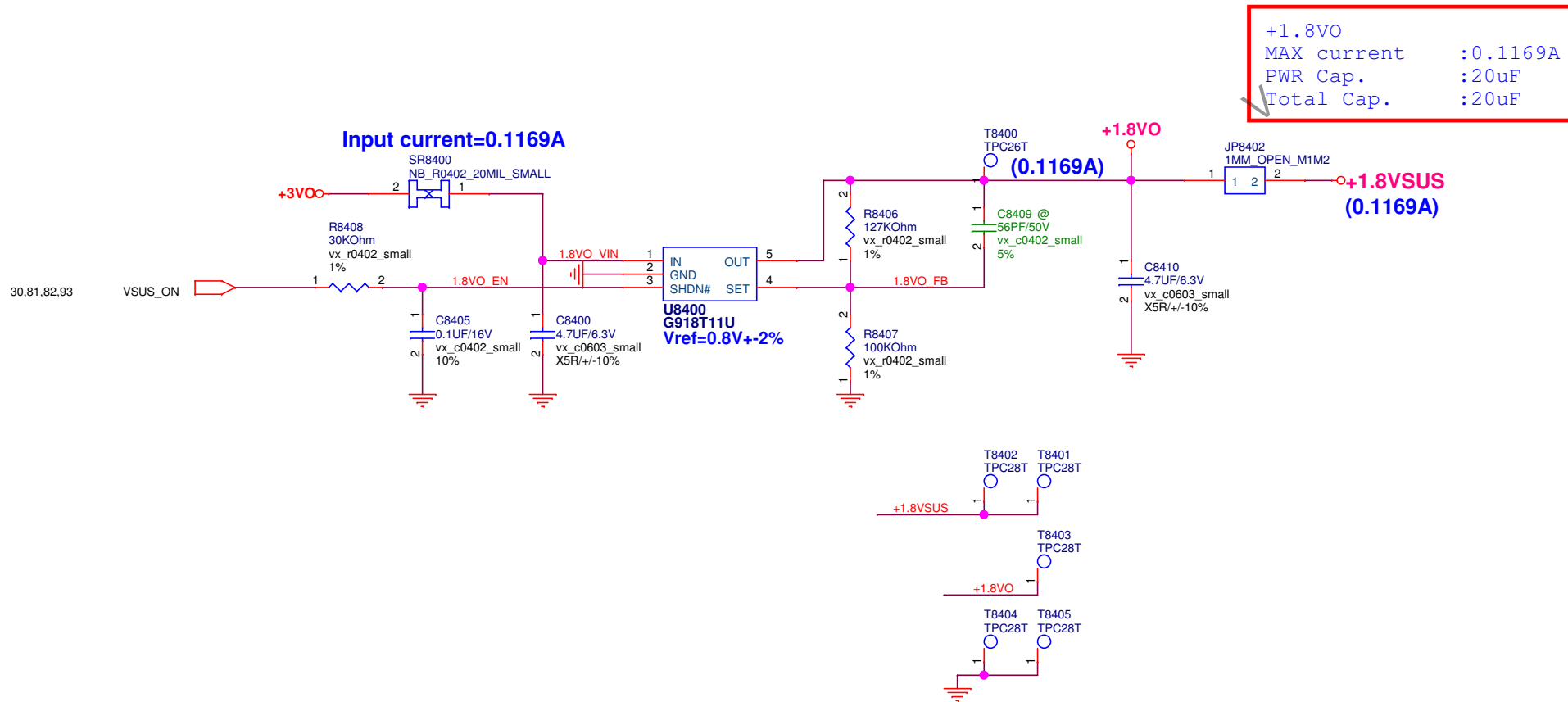
DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

1.8VSUS POWER SUPPLY

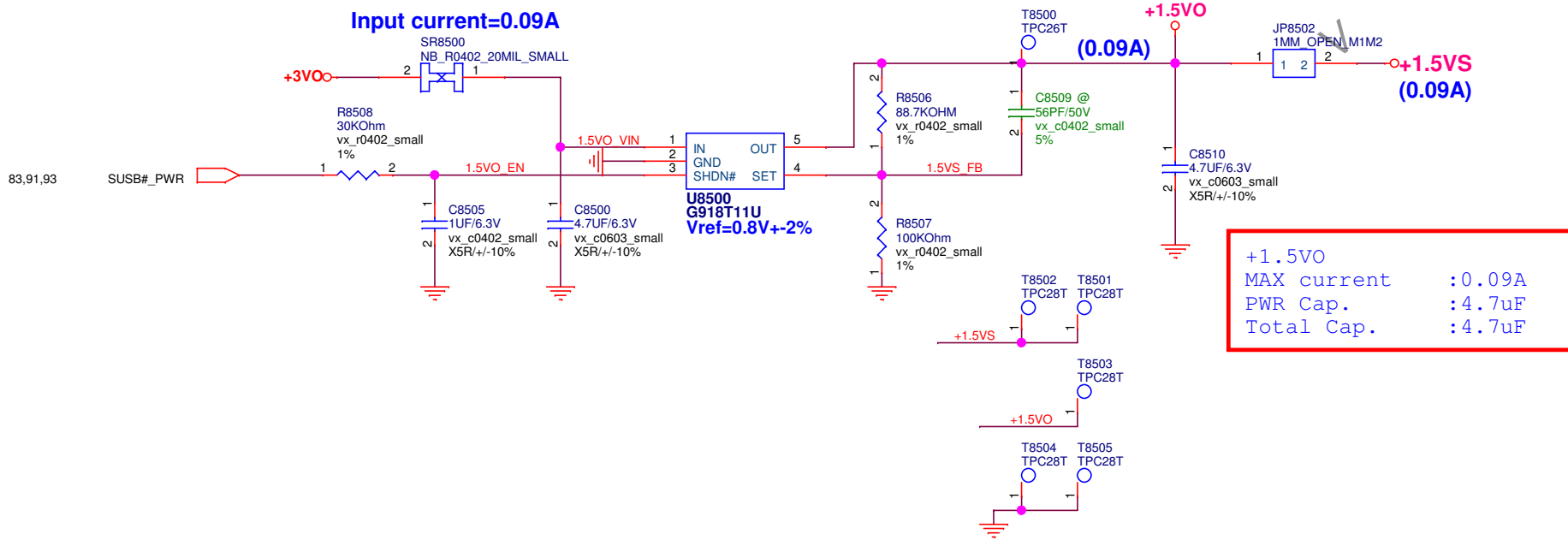


+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF

<Variant Name>

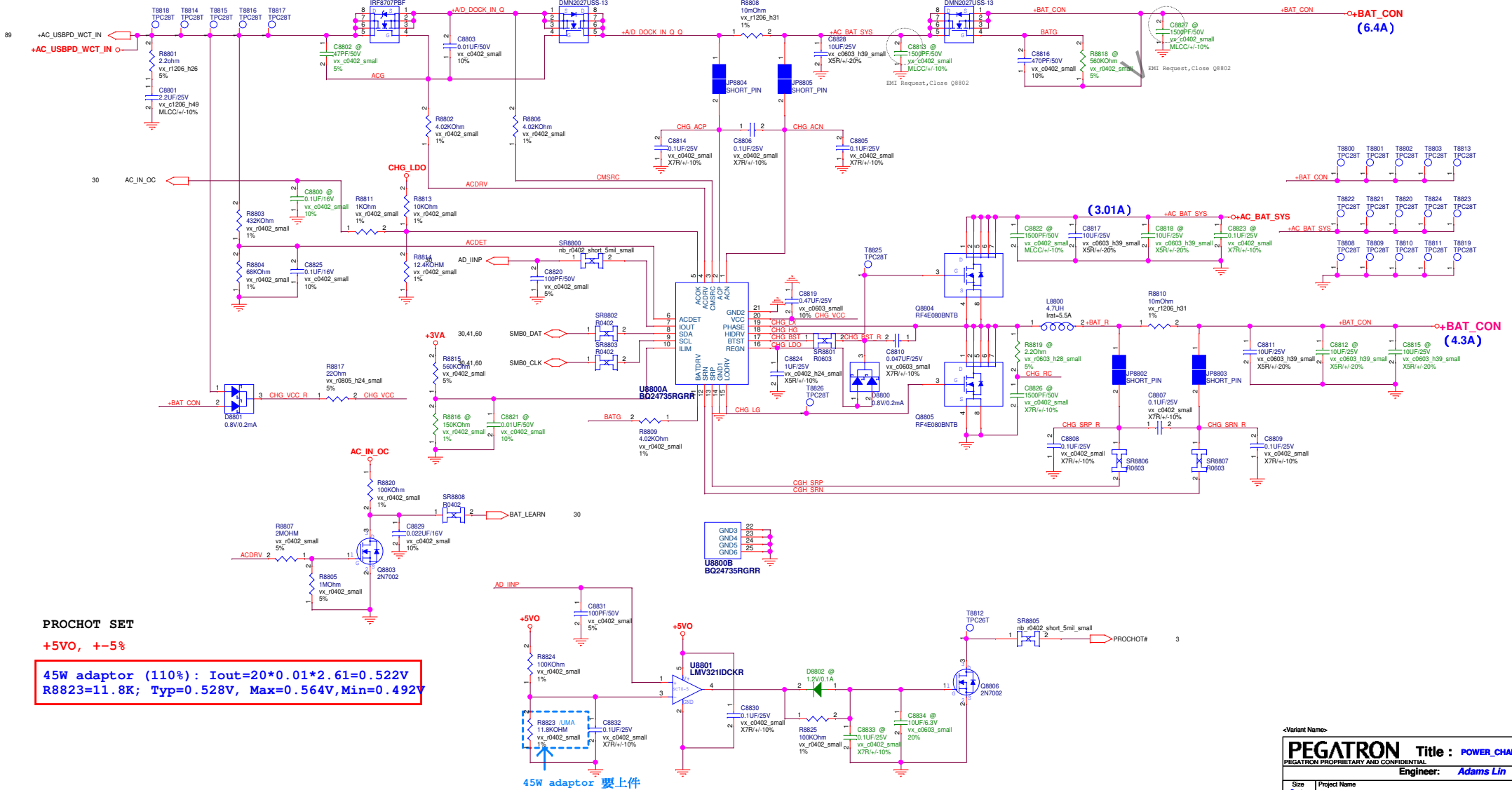
PEGATRON		Title : POWER_+1.8VSUS	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Adams Lin	
Size Custom	Project Name X3		Rev 1.1
Date: Monday, July 11, 2016		Sheet 84	of 94

1.5VS POWER SUPPLY

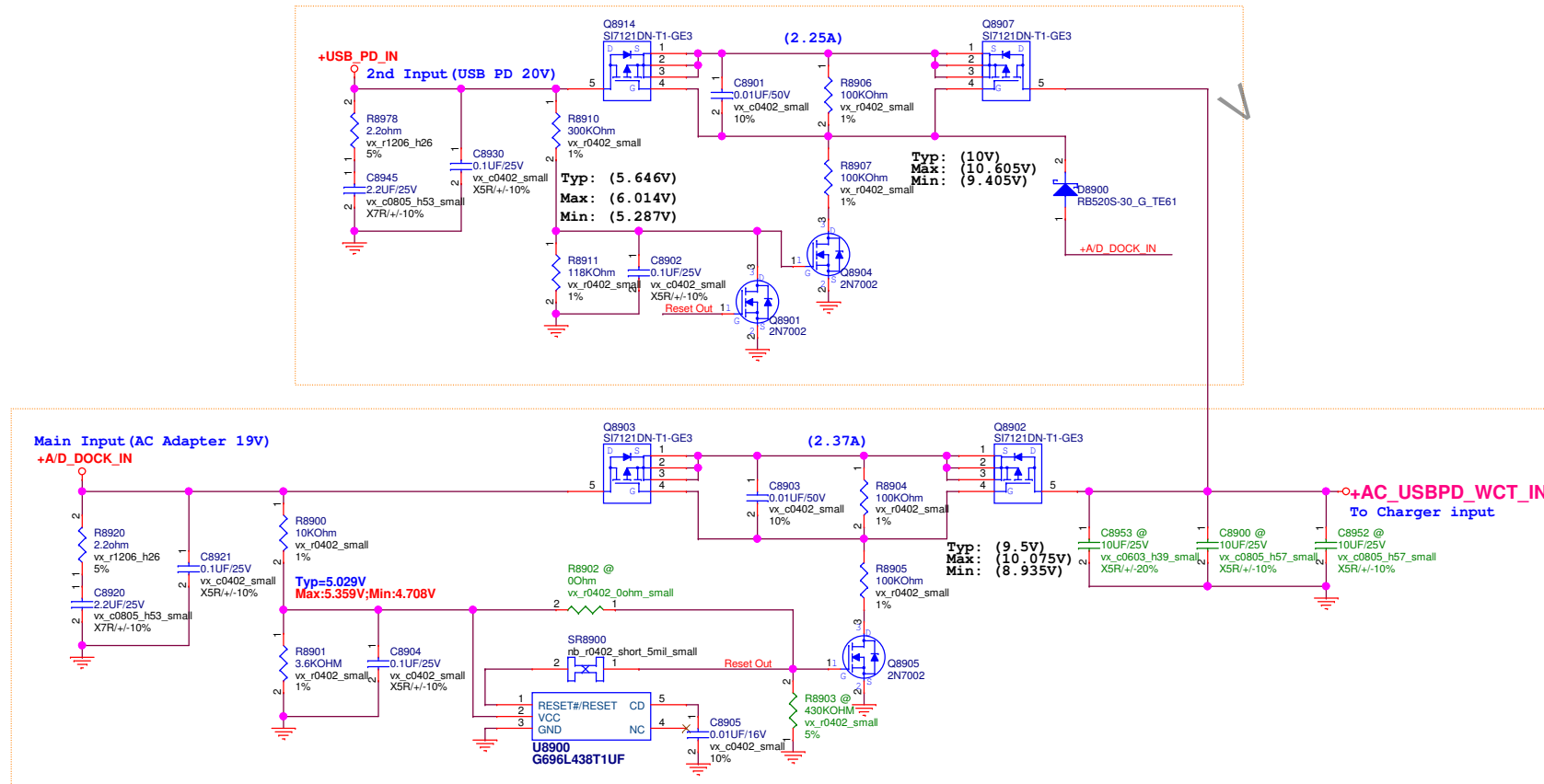


BATTERY CHARGER

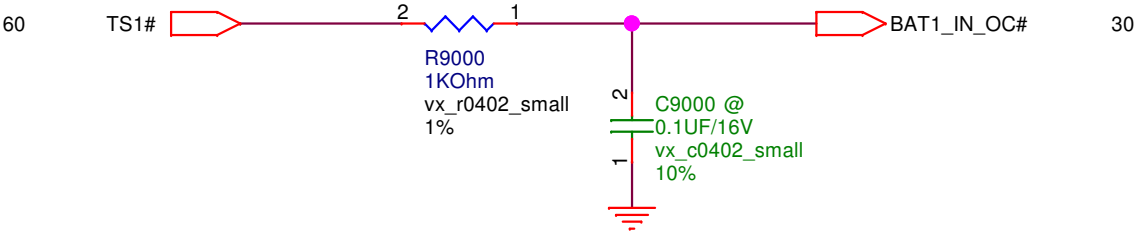
Adapter 65W=3.42A
Adapter 45W=2.37A



2 Input switch Circuit



BATTERY IN DETECT

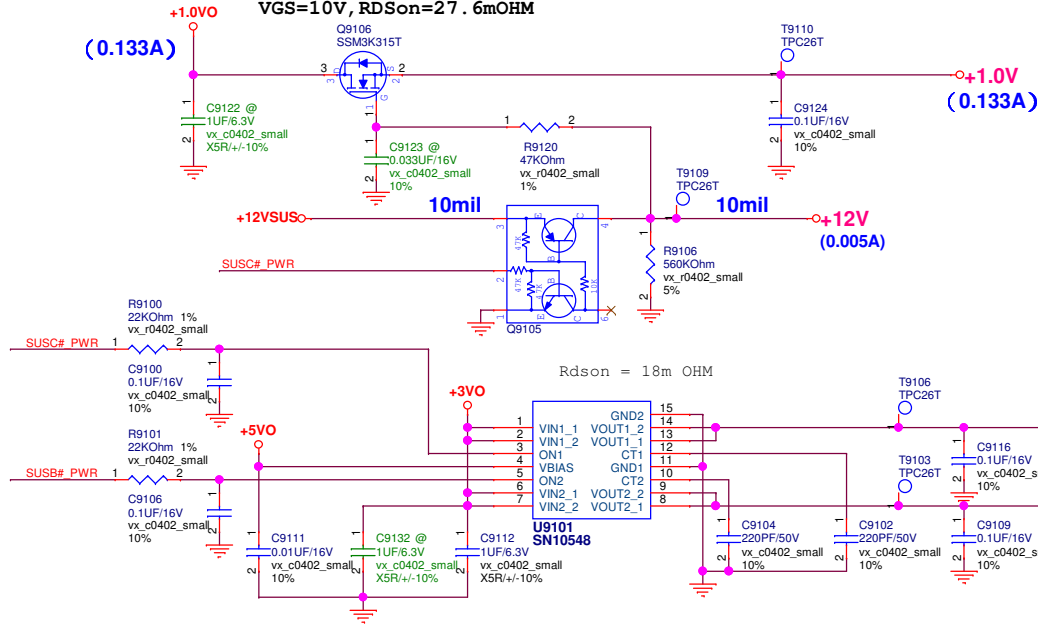


<Variant Name>

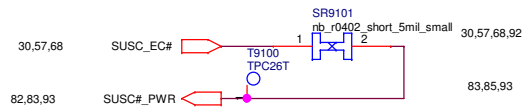
PEGATRON		Title : POWER_DETECT	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Adams Lin	
Size Custom	Project Name X3		Rev 1.1
Date: Monday, July 11, 2016	Sheet 90 of 94		

SUSC#_PWR POWER

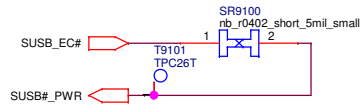
VGS=10V, RDson=27.6mOHM



SUSC#_PWR POWER Control

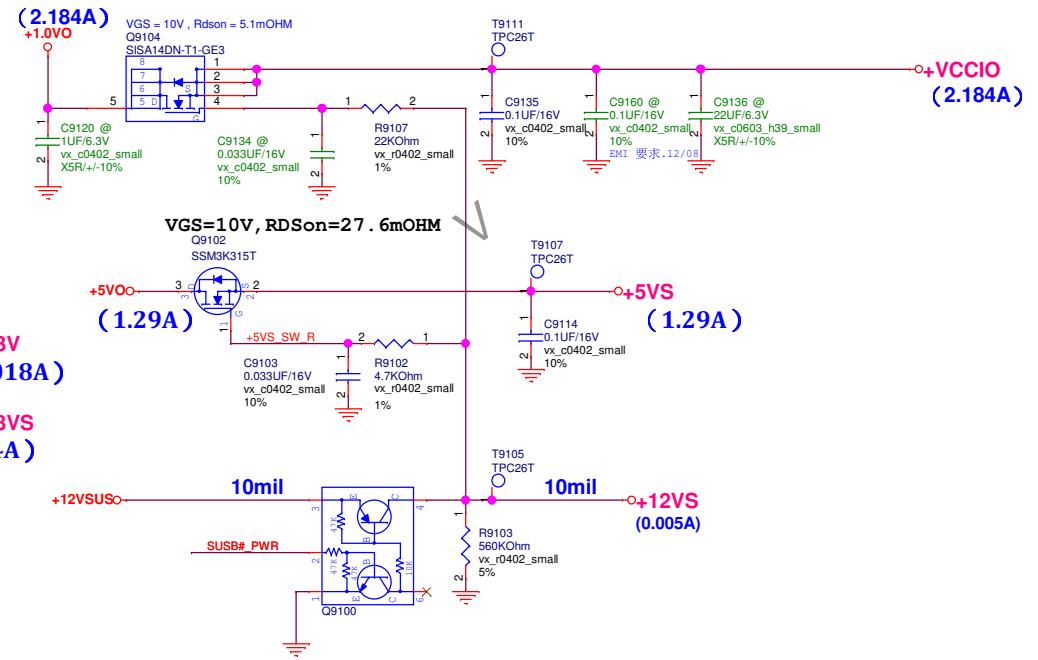


SUSB#_PWR POWER Control



SUSB#_PWR POWER

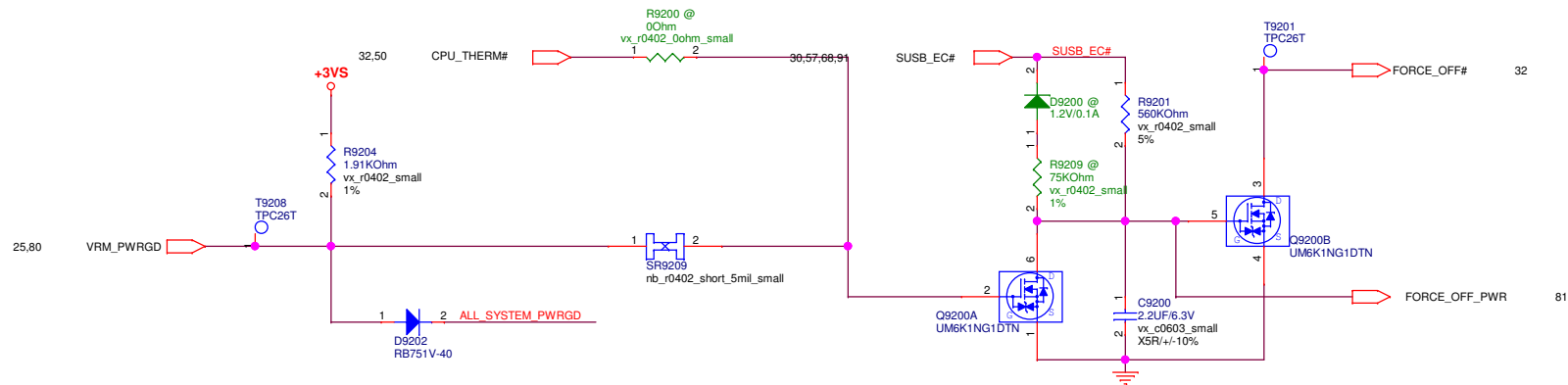
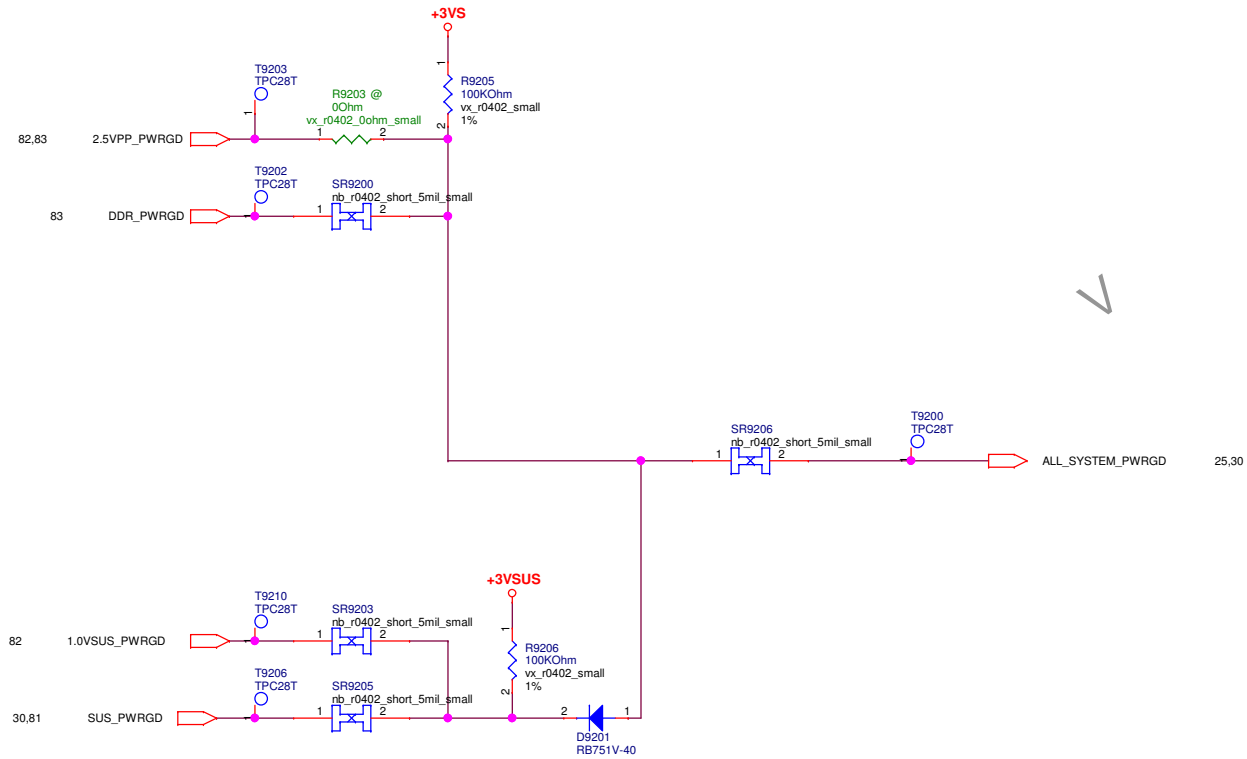
VGS = 10V , Rdson = 5.1mOHM



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Size		Project Name	
Custom		X3	
Date:	Monday, July 11, 2016	Sheet	91 of 94
Engineer:		Adams Lin	
Rev		1.1	

POWER GOOD DETECTOR

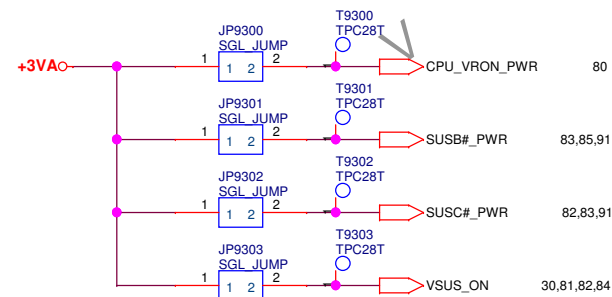


<Variant Name>

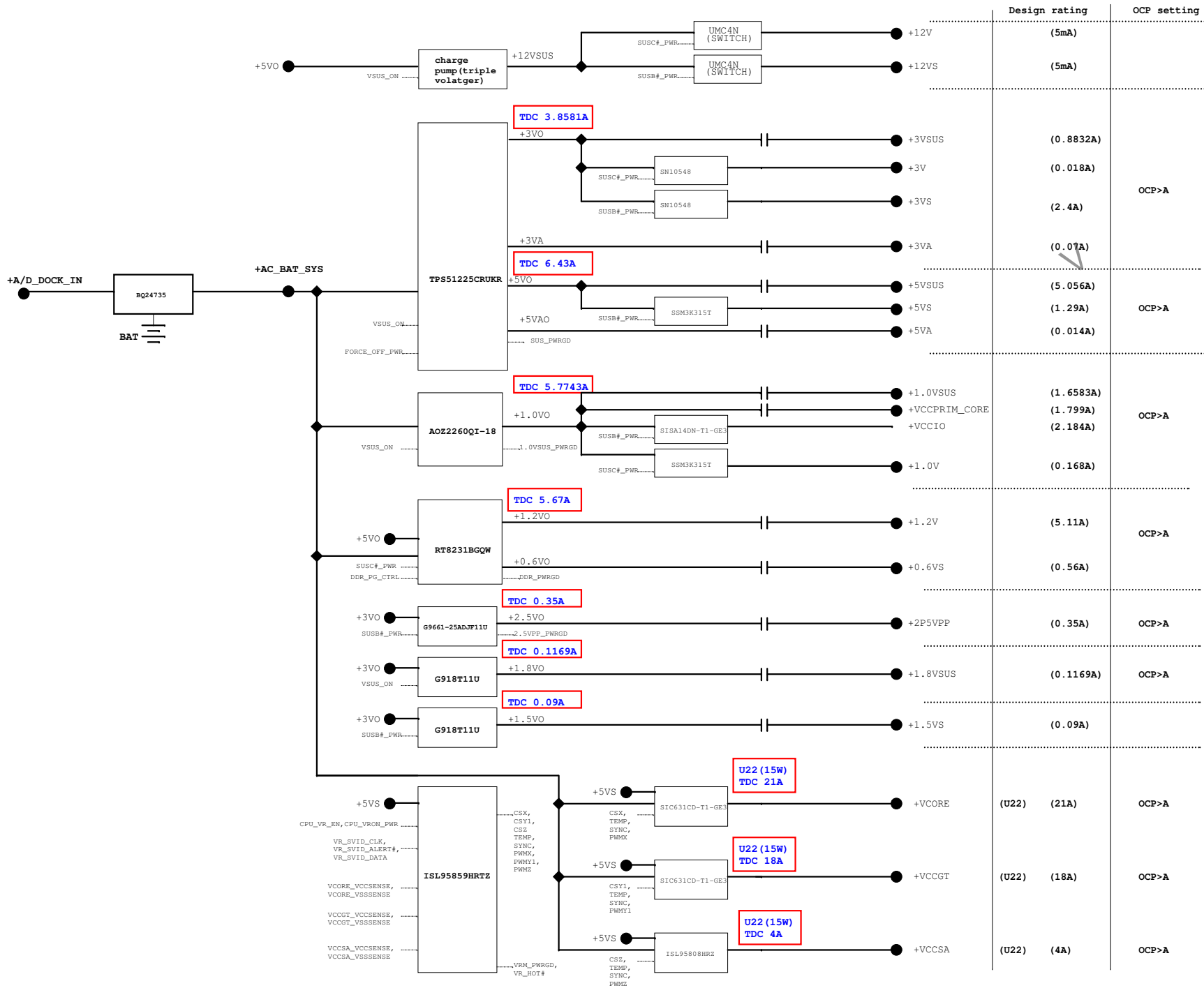
PEGATRON		Title : POWER_PROTECT	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Adams Lin	
Size Custom	Project Name X3	Rev 1.1	
Date:	Monday, July 11, 2016	Sheet	92 of 94

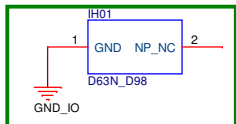
+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	→	+5VO	26,81,82,83,88,91
+3VO	→	+3VO	81,82,84,85,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.2VO	→	+1.2VO	83
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	28,81,91
+5VSUS	→	+5VSUS	41,42,52,56,64,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,22,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	57,91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,19,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	31,48,57,91
+5VS	→	+5VS	31,36,45,48,50,51,57,80,91
+3VS	→	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	→	+0.6VS	15,57,83
+VCORE	→	+VCORE	5,80
+VCCGT	→	+VCCGT	6,80
+VCCSA	→	+VCCSA	7,80
+VCCIO	→	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82

FOR POWER TEST

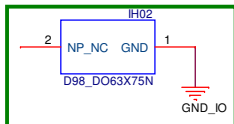


PEGATRON		Title : POWER_SIGNAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-POWER		Engineer: Adams Lin	
Size B	Project Name X3		Rev 1.1
Date: Monday, July 11, 2016	Sheet 93 of 94		



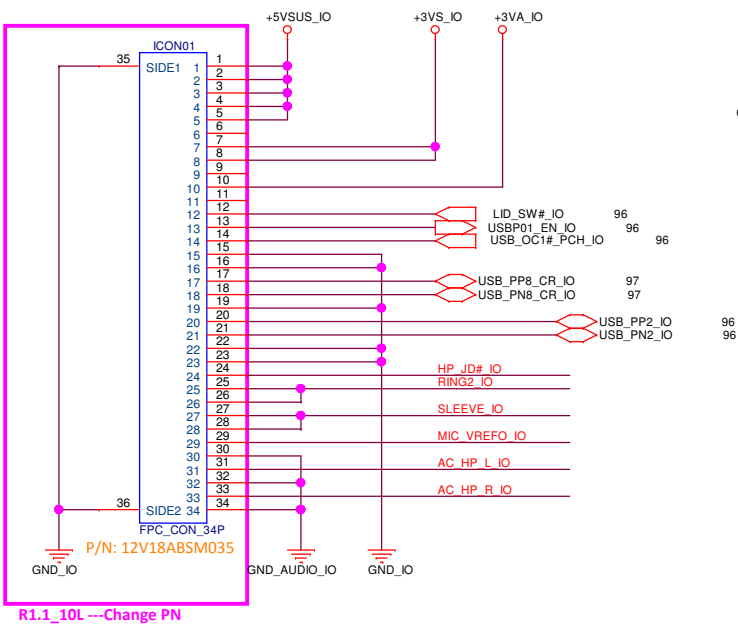
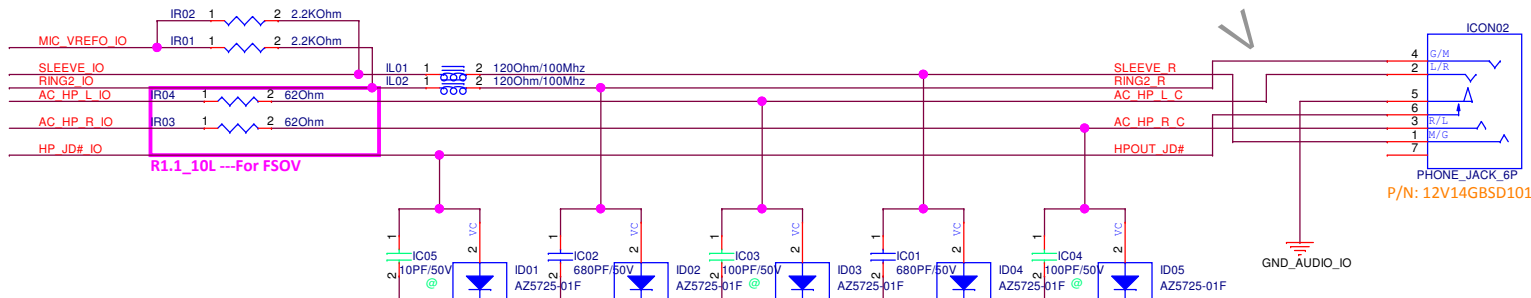


2016.6.6 R1.2_10L ---For ME

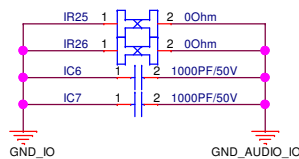


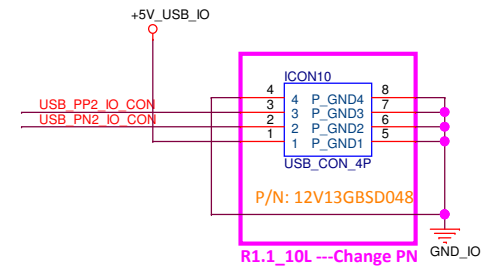
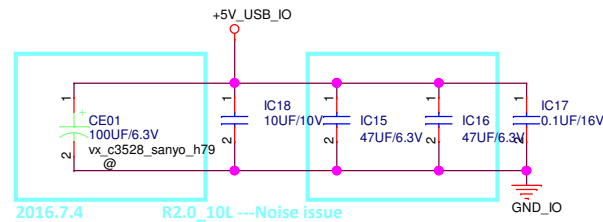
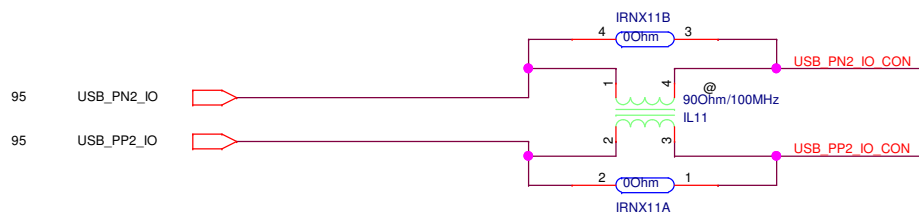
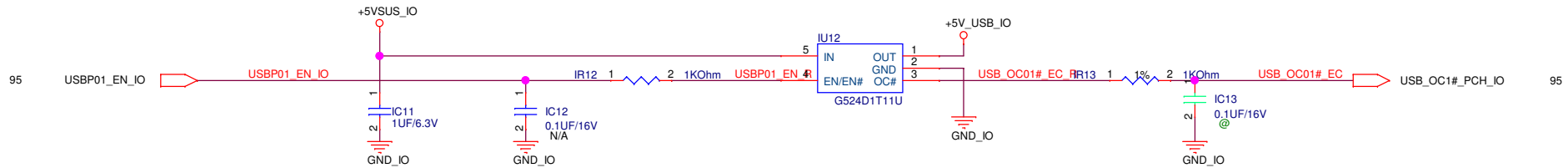
2016.6.6 R1.2_10L ---For ME

AUDIO JACK

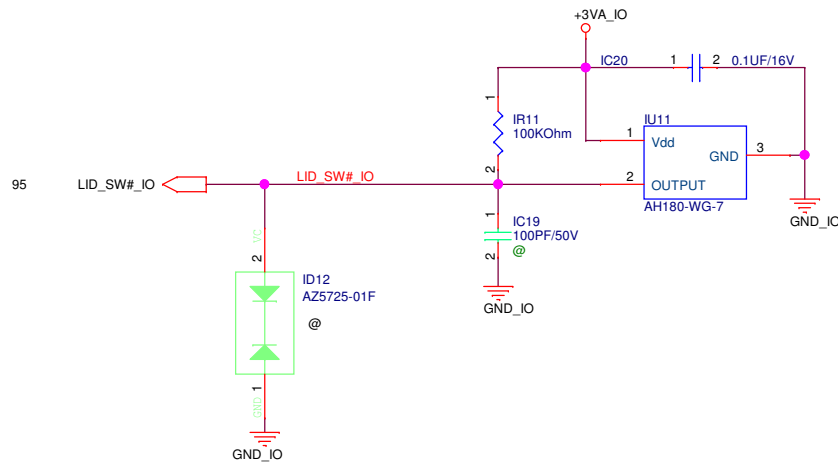
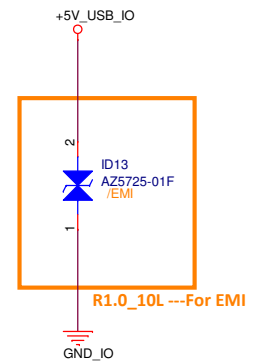
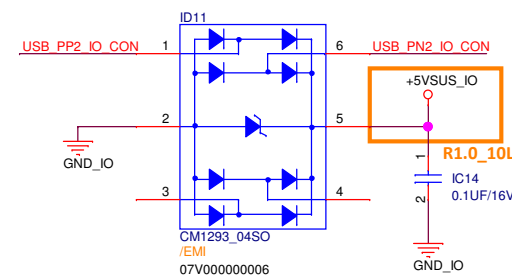


R1.1_10L ---Change PN

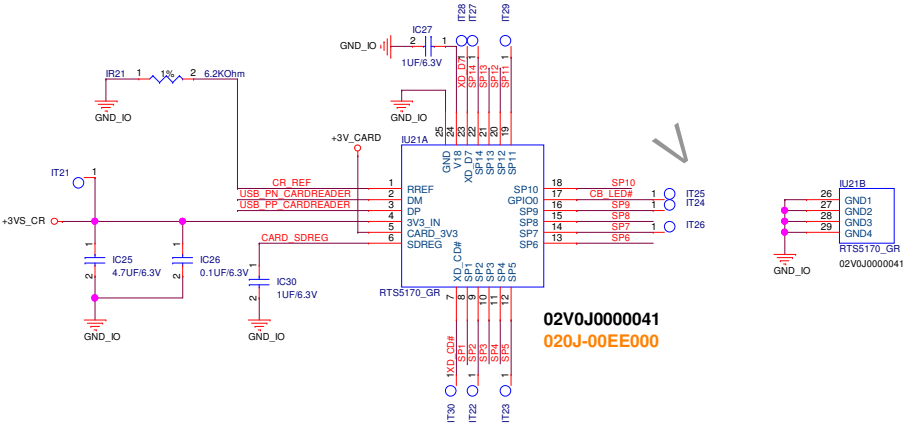
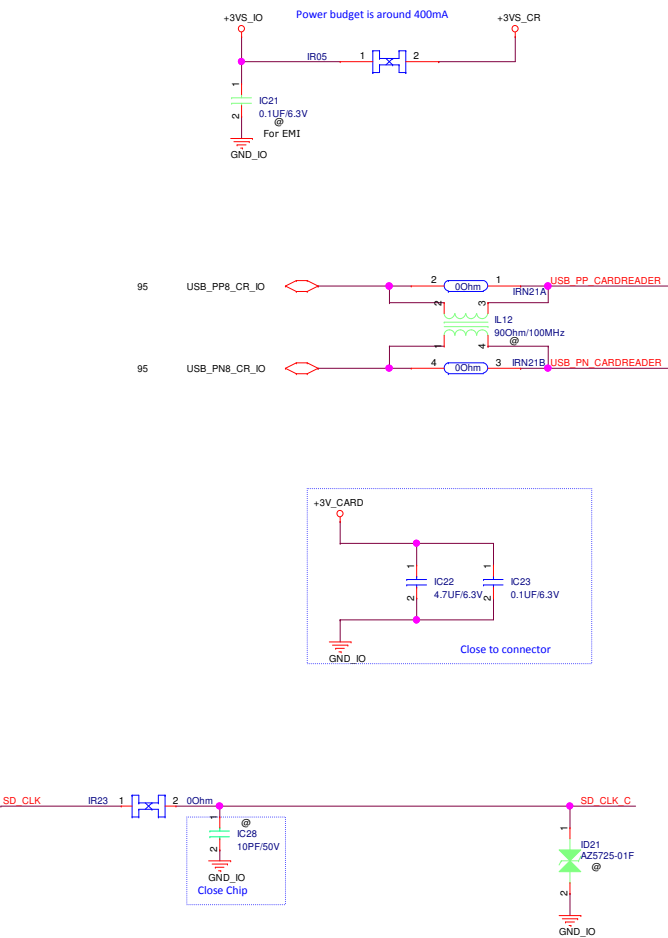




PLACE ESD Diodes near USB Connector



Cardreader



02V0J0000041
020J-00EE000

RTS5170-GR Share Pin Assignment

SP1	SD W/P
SP3	SD D1
SP4	SD D0
SP6	SD C/D#
SP8	SD CLK
SP10	SD CMD
SP12	SD D3
SP13	SD D2